Physical Layer Implementation of a class of ZigBee Baseband Transceiver using FPGA

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Certificate

This is to certify that the work in the thesis entitled ***"Physical Layer Implementation of a class of ZigBee Baseband Transceiver using FPGA"*** by ***Bijaya Kumar Muni*** is a record of an original research work carried out under my supervision and guidance in partial fulfillment of the requirements for the award of the degree of Master of Technolgy (R) in Electronics and Communication Engineering. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

Dr. Sarat Kumar Patra
Professor

To my Parents

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Abstract

ZigBee and IEEE 802.15.4 standard for wireless technology, developed in 2003 were designed for interconnection of data communication using low data rate, low power and low complexity short range communication in a wireless personal area network (WPAN). Later in 2006, it was enhanced for market applicability to remove ambiguities in implementation for low data rate and short range wireless networks with high battery life. This technology supports cost effective, low power, wireless network monitoring and control products based on open global standard.

This thesis presents a FPGA implementation of Baseband physical layer for ZigBee. It presents the designs, implementation, verification and validation.

The ZigBee baseband transceiver proposed in this thesis is based on IEEE 802.15.4 where the transceiver uses OQPSK modulation. DS spread spectrum and half sine pulse shaping is used for coding and baseband processing respectively. The transceiver is initially simulated in matlab software using Simulink and next it was simulated in verilog HDL by the mentor graphics modelsim simulator. Subsequently the baseband transceiver system was realized on Virtex 5 FPGA using ISE design environment.

Further a new form of baseband transceiver was designed using PN sequence generated by Residue number system (RNS). The performance of the transceiver using RNS system was first analyzed through matlab simulation. Following this the transceiver was implemented on Virtex 5 FPGA in ISE design environment.

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Abbreviations

AWGN	Additive white gaussian noise
BER	Bit error rate
CRT	Chinese remainder theorem
CMT	Clock manager tiles
DCM	Digital clock manager
DSCDMA	Direct-sequence code division multiple-access
DSSS	Direct sequence spread spectrum
DU	Data unit
ED	Energy detection
FFD	Full function device
FPGA	Field programmable gate array
GTS	Guaranteed time slot
I-phase	In Phase
I/O	Input/Output
MAC	Medium access control layer
MC/DSCDMA	Multi carrier Direct-sequence code division dynamic multiple-access
OQPSK	Offset quadrature phase shift keying
OSI	Open system interconnect
PHY	Physical layer
PN	Pseudo noise
PPDU	Protocol Data Unit
Q-phase	Quadrature Phase

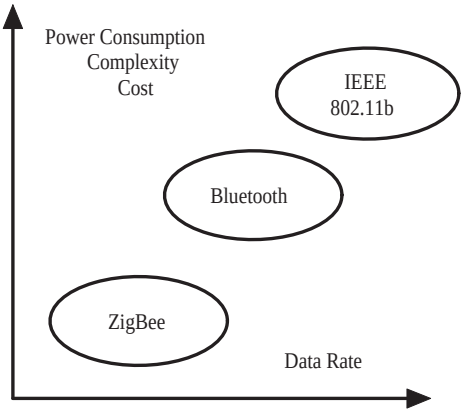
RNS	Residue number system
RFD	Reduced function device
SSP	Security service provider
WPAN	Wireless personal area network
WLAN	Wireless local area network

1

Introduction

Current millennium has seen explosive growth in wireless communication. The short range wireless communication has been used for accessing networks and services without cables, which is a fast-growing technology for providing flexibility and mobility. Major benefits of the technology includes the dynamic network formation, low cost and easy of deployment [1, 2]. There are different protocol standards presented in Figure 1.1 used for the short range wireless communication namely the Bluetooth [3], ZigBee [4] and Wi-Fi [5]. Among these standards ZigBee over IEEE 802.15.4 protocol can meet a wider variety of real industrial needs due to its long-term battery operation, wider useful range and reliability of the mesh networking architecture [6].

ZigBee and Wireless Personal Area Networks (WPANs) are used to transfer short messages like commands of information over a short distance. Like WPAN, ZgBee needs little infrastructure for data exchange. This feature allows the ZigBee alliance group for small, power-efficient and inexpensive solutions to implement in a wide range of wireless devices. So ZigBee alliance group along with IEEE 802.15.4 standard forms the ZigBee protocol networking layers for low data rate short range wireless communication. This standard provides Physical layer(PHY) and medium access control (MAC) specifications for low data rate wireless connection for fixed, portable and moving devices with limited battery



Standards	Data Rate	Typical Range	Applications
ZigBee	20 to 250 Kbps	10 to 100 m	Wireless sensor Network
Bluetooth	1 to 3 Mbps	2 to 10 m	Wireless Headset or Wireless Mouse
IEEE 802.11b	1 to 11 Mbps	30 to 100 m	Wireless Internet Connection

FIGURE 1.1: Short Range Wireless network Comparison

power consumption. Low battery power consumption is biggest advantage of the standard because of the fact that, most of time the network devices are in sleep mode.

1.1 Motivation

ZigBee standard was specifically developed to address the need for very low cost implementation of low data rate wireless networks with ultra low power consumption. The ZigBee Standard reduces the implementation cost by simplifying the communication protocols at reduced data rate. The minimum requirements to meet ZigBee specifications are relatively relaxed as compared to other standards such as IEEE 802.11 and Bluetooth. This reduces the complexity and cost of implementing ZigBee compliant transceivers. This feature of ZigBee enhances the application in wireless sensor network [7] for gathering information from sensors such as temperature,humidity, pressure and other physical parameters.

One of the general trend in research is new implementation strategies for the present technology in real time with an aim to reduce the chip size. For this, FPGA is one of the best hardware tool which is generally used for transceiver implementation [8]. In the literature, several researchers have provided implementation of different part of the ZigBee standard using FPGA [9]. Since VIRTEX 5 FPGA board has wide range of capacity and is popularly used in industry applications for implementation and verification of hardware design. Hence, in this present work the baseband transceiver was implemented on VIRTEX

5 FPGA board.

In fact Direct Sequence Spread Spectrum (DSSS) is used in ZigBee transceiver which uses a PN sequence. In general random PN sequence is used for this purpose. Recently [10] residue number system (RNS) has been used in DSCDMA. This code provides improved performance in terms of better bit error rate. and exhibits better cross correlation. This gives a motivation for implementing RNS based PN sequence for ZigBee transceiver.

1.2 Background of Research

Significant work has been carried out over past few years in the field of FPGA implementation and ASIC implementation for short range wireless communications. This section summarizes some of these.

The advantages of ZigBee in short range wireless communication brought in many researchers trying to implement hardware for real time applications. Oh and Lee [11] implemented a 2.4 GHz radio transceiver for WPAN in $0.18-\mu m$ CMOS technology. In this Offset Quadrature Phase Shift Keying (OQPSK) pulse shaping has been implemented for 2.4 GHz band of IEEE 802.15.4 standard. A circuit implementation of ZigBee transceiver for 868/915 MHz was proposed by Wang *et. al* [12]. The modulator and demodulator for 868/915 MHz band of IEEE 802.15.4 standard have been implemented in [13, 14] for ZigBee wearable devices in medical applications.

The ZigBee standard supports DSSS for baseband modulation [1]. In general Pseudo Noise(PN) random sequence is used in DSSS. However, in ZigBee a standard spreading sequence is used. Recently the RNS based PN sequence has attracted attention of researchers for FIR and IIR filter design [15]. RNS based codes system design can provide implementation with low computational complexity and can be used for efficient architecture for VLSI implementation [16]. It has been demonstrated that, the RNS based PN sequence provides superior performance than PN sequence in DSCDMA [10]. Recently Zhang and Yang [17] proposed a redundant residue number system(RRNS) assisted multi carrier direct-sequence code division dynamic multiple-access (MC/DS-CDDMA) for cognitive radios (CRs). Here

the author have used three types of receiver multiuser diversity aided multistage minimum mean-square error multiuser detector (RMD/MS-MMSE MUD) for signal detection. A 2.45 GHz WPAN modulator and demodulator compliant to IEEE 802.15.4 physical layer has been proposed in [18], where a non coherent demodulation scheme is used to overcome the complexity and power dissipation problem by using phase shift down sampling to detect the maximum phase accumulation, which is the location of correct data. A simulation based study on transceivers using DSSS and OQPSK modulation was investigated in [19] . The bit error rate (BER) performance of the transceiver in additive white gaussian noise (AWGN) and rayleigh flat-fading channels have been analyzed here. A low power baseband processor for IEEE 802.15.4 standard, which estimate and compensate carrier phase error at baseband with carrier phase synchronization has been proposed in [20]. Here an existing packet detection algorithm is used to estimate the large carrier offset. The monitoring of remote controlled switching devices with power management system using ZigBee is presented in [21]. A low power 2.4 GHz radio transceiver consuming 14.7 mA current in receive mode and 15.7 mA in transmitting mode with Packet Error Rate(PER) of 1% has been designed by Kluge et.al in [22]. A low cost demodulator for ZigBee receiver which extracts the symbol directly from the baseband signal rather than recovering the PN sequence was presented [23].

1.3 Objective of Thesis

The work focuses in this thesis is to design and implement of ZigBee baseband transceiver for IEEE 802.15.4 for short range wireless communication system. The design is preferred to use in wireless sensor network applications as per the customer requirement, like in industry automation, medical applications and military applications etc.

The work reported in this thesis was primarily carried out as a part of design for defence application. It was designed to develop a ZigBee transceiver based on IEEE 802.15.4. The RF section design of this ZigBee transceiver was completed in [24]. This thesis presents the baseband processing of ZigBee transceiver. The objectives of this thesis involved in

design includes.

- Simulation of the ZigBee transceiver system using MATLAB/SIMULINK
- Hardware description language verilog HDL based design and simulation in modelsim simulator.
- Implementation of the design in VIRTEX 5 FPGA board.
- Design a new form of baseband transceiver using new set of PN sequence based on residue number system(RNS).
- Analyze the performance of the RNS based baseband transceiver with pseudo noise(PN) sequence based ZigBee transceiver in AWGN channel and Rayleigh fading single path channel.
- Verilog HDL simulation of RNS based baseband transceiver using modelsim simulator.
- Implementation of RNS based design on VIRTEX 5 FPGA board.

1.4 Thesis Organization

This section presents the outline of the thesis.

The thesis has been divided into five chapters, remaining four chapters are described here.

Chapter-2: ZigBee for IEEE 802.15.4 Standard

The basic of IEEE 802.15.4 standard for short range wireless communication is described briefly. The ZigBee protocol's networking layer and the network topologies used in ZigBee are presented. Various type of data transfer techniques like beacon enabled and non-beacon enabled along with the physical layer specifications of IEEE 802.15.4 are described. The modulation scheme used in ZigBee baseband transceiver is also discused in this chapter.

Chapter-3: FPGA Implementation of ZigBee Baseband Transceiver

The FPGA implementation scheme for ZigBee transceiver is explained in this chapter. ZigBee baseband transmitter and receiver are first designed in hardware programming language verilog HDL and simulated in modelsim simulator. The transmitter consists of bit to symbol, symbol to chip, serial to parallel blocks and pulse shaping circuit are described and each of these blocks are simulated on modelsim. Following this the deign has been implemented on VIRTEX 5 FPGA Board. In similar manner the receiver consists of parallel to serial conversion, correlation of received data bit and decoding blocks. All the blocks are first simulated on modelsim simulator and next implemented on VIRTEX 5 FPGA board. The chapter covers the details of VLSI module of transceiver, clock circuit generator and input output description of each module. Detail description of digital clock manager(DCM) is also presented.

Chapter-4: ZigBee Transceiver Design using Residue Number System based PN sequence for Spreading

Design of a new ZigBee transceiver using a new set of PN sequence based on Residue Number System(RNS) is proposed in this chapter. The transceiver uses these codes for spreading and despreading. The chapter presents brief description of RNS which includes the basics of RNS , moduli-set selection, Chinese Remainder Theorem (CRT) etc. The chapter presents the performance of RNS based PN sequence in ZigBee. The bit error rate performance of the transceiver is compared with standard ZigBee BER performance. Following this the proposed PN sequence is used for DSSS in the transceiver.

Chapter-5: Presents conclusion and Future scope of work. The chapter provides an analysis on contribution of the work reported in this thesis. Limitation of work and some direction for future work is also presented here.

2

ZigBee for IEEE 802.15.4 Review

2.1 Introduction

ZigBee standard provides a set of specifications for short range wireless communication with low battery power consumption, in mesh networking topology. This enables applications to work in remote areas without intervention. One such application is sensor network, which can monitor patients health condition by a physician who is away from the patient and patient can be in remote area. The patient wears a ZigBee device which in turn is interfaced with a ZigBee sensor [25, 26]. The ZigBee sensor collects information of patients health parameters like blood pressure, pulse rate, sugar etc and sends this information to personal computer placed inside patient's cabin with the help of ZigBee protocol from where the information transferred to the physicians through broadband internet connection [2, 14].

Wireless ZigBee sensors have been used to detect the structural strength of large building by placing ZigBee enabled wireless sensors at different part of the building [27]. All the sensors combining to form a ZigBee wireless network and are able to gather the structural information of the building on periodic basic. It helps the authority of the building for inspection of structural strength of the building before opening to the public after a disaster like earthquake or tsunami etc[28].

Table 2.1: ZigBee Terminology in contrast to IEEE 802.15.4

ZigBee Terminology	**IEEE 802.15.4 terminology**
ZigBee Coordinator	IEEE 802.15.4 PAN Coordinator
ZigBee Router	IEEE 802.15.4 Coordinator(FFD)
ZigBee end device	Reduced function device(RFD)

There are many standards developed for the collection of information from different source point. This includes short range wireless networking standards like IEEE 802.11[29] wireless local area network (WLAN), Bluetooth [30]. Each standard has its own advantage for particular field of application. For short range, low data rate and very low power consumption with low implementation cost the ZigBee standard is most suitable.

2.2 ZigBee Data Communication

To enhance data communication, the ZigBee network uses mesh topology, IEEE 802.15.4 network devices like Reduced Function Device (RFD), Full Function Device(FFD) and various data transfer techniques such as beacon enabled and non-beacon enabled etc. In ZigBee data communication IEEE 802.15.4 devices plays major role which are termed as ZigBee devices. The ZigBe standard terminology used in the network is presented at Table 2.1.

2.2.1 ZigBee Network Device

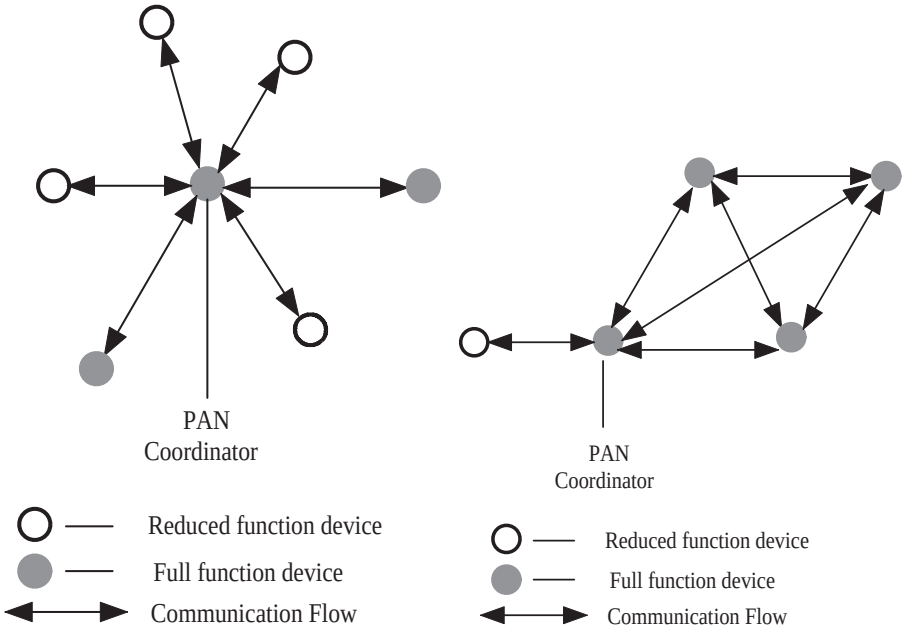
A full function device (FFD) can perform all the tasks and responsibilities mentioned in IEEE 802.15.4 standard and can play any role in the network topology. A FFD acts as master to all of the RFDs associated with the network designated as coordinator and can communicate with any device in the network [31, 32].

A FFD can act as three different types of role such as a coordinator, a PAN coordinator and a device. A coordinator in a network must be a FFD having the capability of relaying message from FFD to RFD. The coordinator can be referred as PAN coordinator if it is the principal coordinator of the network. And the device in the network other than coordinator is known as device [4].

The capability of reduced function device (RFD) is limited in the standard. The applications of RFD are for simple applications like turning on and off switches etc. The RFD can communicate with a full function device only not with any other RFD. The reduced function device has normally less power as compared to full function device (FFD).

2.2.2 Topologies in ZigBee

As per the requirement of application IEEE 802.15.4 operates in two types of topology such as star topology and peer to peer topology. The Figure 2.1a shows star topology and Figure 2.1b shows peer topology of formation of ZigBee network.



(a) Star Topology (b) Peer Topology

FIGURE 2.1: Star and Peer to peer Topology

- Star topology

  In star topology the communication is established between the full function device (FFD)and all other reduced function devices. An FFD activated first time will establish its network with the RFDs and becomes PAN coordinator. The PAN coordinator

starts a network chooses a PAN identifier which is currently not used by any other network. This allows independent operation of star network [32].

A PAN coordinator facilitates some associated application to initiate and terminate the network communication so it is used to initiate, terminate and routing of communication around the network, for which PAN coordinator is considered as the primary controller of the PAN. The network devices operating on a network have unique 64-bit addresses which is used for identification of the device. This address may be used for direct communication within the PAN, or a short address can also be allocated by the PAN coordinator when the device associates with the network [1].

Mostly the PAN coordinator gets supply from a main supply but all other RFD are as usually battery powered. This topology mainly applied for home automation, personal computer peripherals, different games and toy application.

- Peer to peer topology

  Peer to peer topology is different from star topology. In this topology the devices can communicate with each other as long as they are in the range of the network. The device which first communicates to the network termed as PAN coordinator, constructs the network structure formation and also restricts the topological formation of network. Peer to peer topology can be help full for creating larger topology or formation of mesh topology by connecting the star topologies each other along with peer to peer topology. Application of peer topology lies in industrial control and monitoring, wireless sensor network, asset tracking and for security purposes.

- Mesh topology

  Mesh topology is the combination of many star topology and peer to peer topology. In ZigBee standard mesh topology of the network is helpful to create a ZigBee cluster as presented in Figure 2.2 [2]. This topology helpful to create cluster tree network where most of the devices use FFDs for allowing other devices to associate with the network.

In a network, RFDs are used as end device as RFD does not allow other device to associate with network due to its limited resources. Out of all FFDs one FFD acts as PAN coordinator, which first initiates the network by choosing an unused PAN identifier and broadcasts beacon messages to neighbor devices. The device receiving beacon message can request the PAN coordinator to join the network, if the PAN coordinator permits the device to join it adds a new device as a child device in its neighbor list. Then the new device adds the PAN coordinator as its parent in its neighbor list and begins transmitting periodic beacon messages. Other new devices can join the network with that device. If the original candidate device unable to join the network at the PAN coordinator then it will search for another PAN coordinator [4].

2.3 IEEE 802.15.4 Physical Layer Specifications

2.3.1 Introduction

IEEE 802.15.4 specifies the physical layer protocol functions and interactions with MAC layer which defines the hardware level requirement such as jamming resistance, receiver sensitivity and transmitter output power etc. Physical layer of ZigBee networking protocol layer performs following tasks.

- Activation and deactivation of the radio transceiver.
- Energy detection(ED) with in the current channel.
- Link quality indicator for received packets.
- Clear channel assessment (CCA) for carrier sense multiple access with collision avoidance (CSMA-CA).
- Channel frequency selection.
- Data transmission and reception.

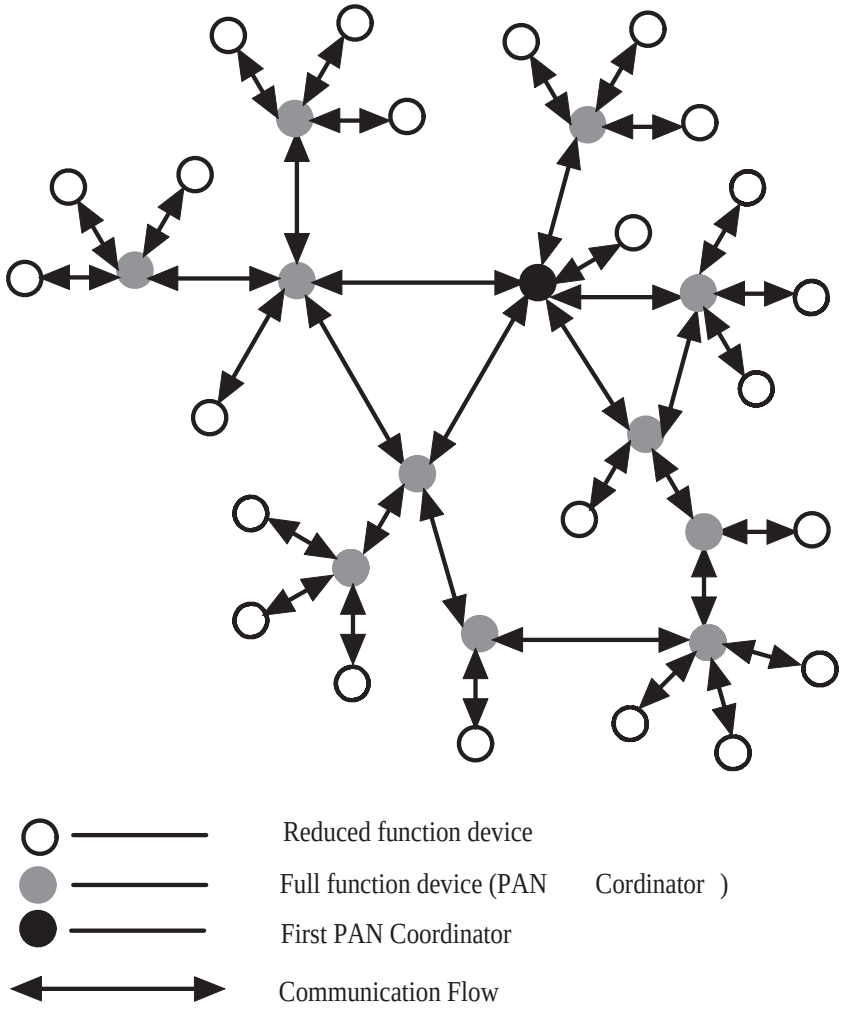


FIGURE 2.2: ZigBee Cluster Tree

- Energy detection

  In ZigBee network if a device need to transmit signal message then it first goes to receive mode to detect the signal energy in the desired channel. This process is known as energy detection(ED). For 2.4 GHz the signal energy spread over eight symbol periods. In this process the receiver estimates the signal energy level not the type of signal. The Energy detection process unable to detect the weak signal with lower energy level close to receiver sensitivity level. Hence the receiver sensitivity energy level is chosen to be lowest signal energy to detect the weak signal of lower

energy with a packet error rate of less than 1%. After this process the MAC layer requests the PHY layer to perform energy detection then the PHY layer returns an 8-bit integer representing the energy level of the desired frequency channel of interest.

- Carrier sense(CS)

  Carrier sense technique is used to verify the availability of the channel for communication or method of free channel detection in network. Similar to ED here also the device wants to transmits data first goes to receive mode to identify whether any signal is present in the desired frequency channel. In CS the signal is demodulated to verify whether the signal modulation and spreading are compliant with the characteristics of the PHY that is currently in use by the device. If the signal in the channel is compliant to the IEEE 802.15.4 PHY than the device considers the channel is busy even if the energy level is high in the channel.

- Link Quality Indicator(LQI)

  Link quality indicator is a parameter which indicates the quality of data packets received by the receiver. The quality of packets can be found by the measurement of received signal strength (RSS), which in turn is the measure of total energy of the received signal. Quality or error in data packets can also be found out by the measurement of signal to noise ratio (SNR). Higher the SNR value lower the chance of error in data packet or vice versa as mentioned by (2.1).

$$SNR = Total\ Signal\ power(P_S)/Total\ Noise\ power(P_N) \tag{2.1}$$

  LQI is performed for every data packet received by the receiver, and the LQI information is reported to the MAC sub layer by using a response. The LQI information is also available to the network and application layer of the architecture which is used for data path selection. Network layer can use the LQI values of the device in the network to decide the path to route a message. The path has higher LQI values have better chance of reception of message by the receiver.

- Clear channel assessment(CCA)

  CCA is a part of PHY layer management service which performs in first step of CSMA-CA. MAC layer requests PHY layer to perform clear channel assessment which ensures that the channel is free. In CCA the results of Energy Detection (ED) and carrier sense (CS) decides whether the channel is assumed to be free or not. CCA is performed in following three modes.

- Mode 1

  In this mode of operation, the Energy detection result considered to detect the usage of frequency channel. If energy level is above the ED threshold, channel is considered as busy. Here the ED energy threshold is set by the device manufacturer.

- Mode 2

  In this mode the carrier sense (CS) result taken in to account for checking the availability of free channel. Here the channel is busy only if information in frequency channel is compliant of PHY layer of the device that is performing CCA.

- Mode 3

  This is the hybrid of Mode I and Mode II, where the combination of mode I and mode II are performed as logically OR and logically AND as given below.

  (i) The detected energy level is above the threshold and the carrier in the channel is sensed. (ii) The detected energy is at above the threshold or carrier in the channel is sensed.

2.3.2 Data rate and frequency of operation

There are three bands of operating frequency for ZigBee. They are 868 MHz, 915 MHz, and 2.4 GHz band. Since 2.4 GHz frequency band is available world wide, the 2.4 GHz band is widely used for short range wireless communication. 868 and 915 MHz band are

Table 2.2: Data rate and frequency of operation

Frequency(MHz)	Number of Channels	Modulation	Chip Rate (Kchips/s)	Bit Rate	Symbol Rate (Ksymbol/s)	Spreading Method
868-868.6	1	BPSK	300	20	20	Binary DSSS
902-928	10	BPSK	600	40	40	Binary DSSS
2400-2483.5	16	O-QPSK	2000	250	62.5	16-array Orthogonal

Table 2.3: IEEE 802.15.4 Channel assignment

Channel Page	Channel Number	Description
0	0	868 MHz band (BPSK)
	1-10	915 MHz band (BPSK)
	11-26	2.4 GHz band (O-QPSK)
1	0	868 MHz band (ASK)
	1-10	915 MHz band (ASK)
	11-26	Reserved
2	0	868 MHz band (O- QPSK)
	1-10	915 MHz band (O-QPSK)
	11-26	Reserved
3-31	Reserved	Reserved

respectively used in Europe and North America. The specifications for different band of operation is given in Table 2.2.

2.3.3 Channel Assignment

The initial release of IEEE 802.15.4 2003 version did not include channel pages. In initial release there were provision of more than 27 channels, so it can exceeds up to 32channels. To support the growing number of channels channel assignment were defined through combination of channel number and channel pages in IEEE 802.15.4 2006 version. In IEEE 802.15.4 standard the channel page 0-2 are used for 868/915 MHz and 2.4 GHz bands and channel page 3-31 are reserved for future extension of channel number[1]. To distinguish between the supported PHYs channel pages are introduced in the current release as presented in Table 2.3.

By using the above table the center frequency of different bands are calculated

- Center frequency for 868 MHz band

$$f_c = 906 + 2 \times (Channel\ Number - 1) \tag{2.2}$$

by using (2.2) the center frequency for channel number 4 can be calculated to be 912 MHz.

- Center frequency for 2400 MHz band

$$f_c = 2405 + 5 \times (Channel\ Number - 11) \tag{2.3}$$

by using (2.3) the center frequency for channel number 12 calculated to be 2410 MHz.

2.3.4 ZigBee protocol Architecture

Figure 2.3 shows ZigBee Networking protocol Layers [2]. Out of seven layers of OSI architecture ZigBee implements the layers which are essential for low power, low data rate applications. In ZigBee architecture the lower two layers ie Physical layer (PHY) and medium access control (MAC) are defined by IEEE 802.15.4 and all other layers are defined by ZigBee. The security features are defined by both ZigBee and IEEE 802.15.4 standard. The network architecture that implements all layers as shown in Figure 2.3 is known as ZigBee protocol networking layers. The layer to layer communication takes place with the help of service access points (SAP), which are the mutual points in the architecture at which one layer can requests the services of another adjacent layer and after getting the request the SAP forwards the request to next layer. The role of service access points(SAPs) in ZigBee protocol architecture are as follows.

- NLDE-SAP(Network Layer Data Entity Service Access Point) Application layer unit or APS Security Management requests data service to network layer.

- NLME-SAP(Network Layer Management Entity Service Access Point) Application layer device Management unit can request any management request to network layer by this SAP.

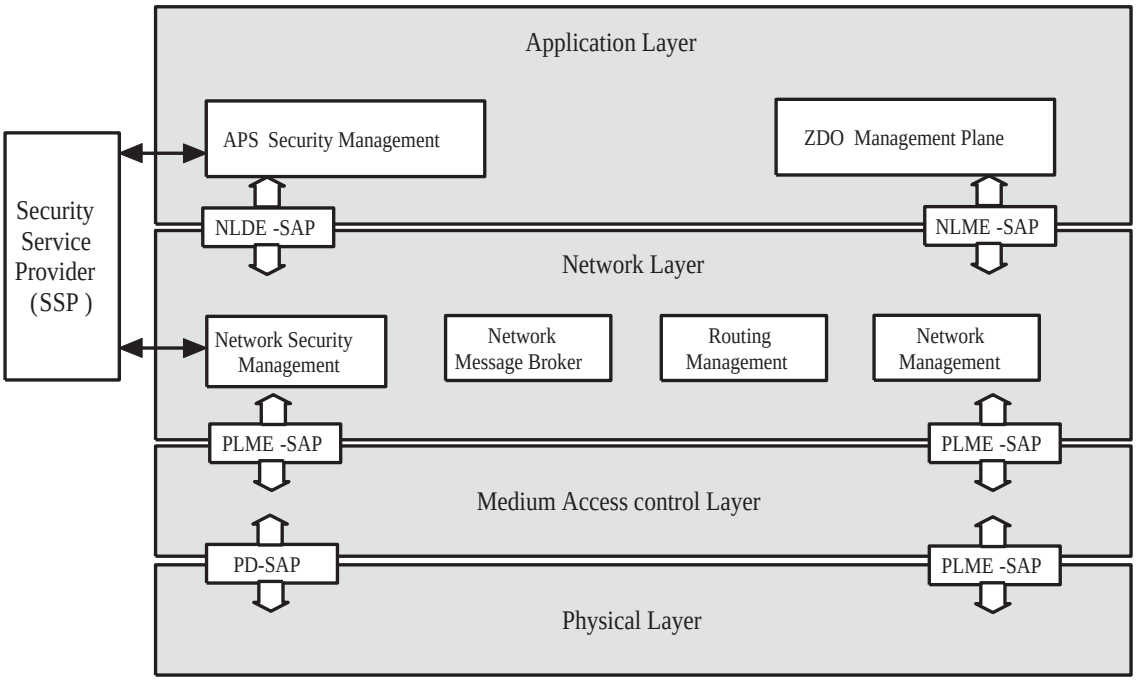


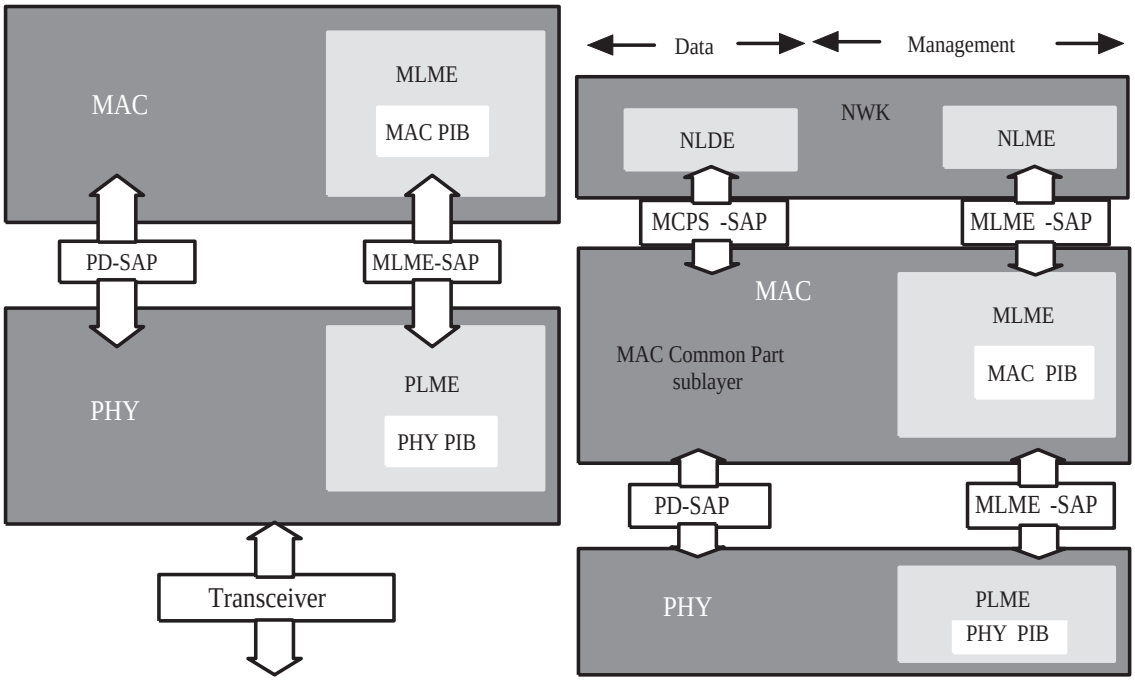
FIGURE 2.3: ZigBee Protocol Layers

- MLDE-SAP(MAC Layer Data Entity Service Access Point) Network Layer requests any data service from MAC.
- MLME-SAP(MAC Layer Management Entity Service Access Point) Network management entity requests to this SAP for any control service from MAC layer.
- PD-SAP(PHY Data Service Access Point) The MAC layer requests any data service from PHY layer
- PLME-SAP(Physical Layer Management Entity Service Access Point) The MAC layer requests for any control services from PHY layer.

2.3.5 PHY Layer Services

Physical layer is an intermediate stage between MAC layer and the ZigBee transceiver. This layer includes two type of services such as PHY data service and PHY management service. PHY data service is responsible for transmission and reception of PHY protocol

data unit (PPDU) across the radio channel which is accessed through service access point PD-SAP. PHY management entity is known as physical layer management entity (PLME) which provides the layer management services to MAC and is accessed through PLME-SAP. PHY layer also maintains a database of objects associated with PHY layer which is called as PHY information data base ((PIB).



(a) PHY Reference Model Interferences MAC (b) MAC sub layer reference model

FIGURE 2.4: PHY and MAC Reference Model

PHY Data Service

The local MAC layer generates a requests for transmission and provides MAC Protocol Data Unit(MPDU) which is transmitted to PHY layer. After getting request from MAC, PHY process the request and acknowledges to MAC layer with a report of successful or unsuccessful transmission containing following information. The PHY reference model for interfacing MAC is shown in Figure 2.4a. Once the data is received by radio transceiver then the PHY layer notifies the MAC layer for arrival of MPDU along with the LQI information.

The reason of unsuccessful transmission:

- The radio transceiver may be in receiving mode, it should be in transmitting mode because the radio transceiver unable to transmit and receive simultaneously.
- The radio transmitter may be busy for transmitting. (It is assigned with one task of transmission)
- The Radio transceiver may not be in enable state, it is in disable state.

PHY Management Services

PHY management services are performed by Physical Layer Management Entity Service Access point (PLME-SAP). The PLME-SAP is used to transport management commands between PHY and MAC. PLME-SAP performs following tasks [1].

- Clear channel assessment: When CSMA requires a channel access the MLME requests PLME for CCA and the results of CCA can be (i) transceiver disabled (ii) channel is available for communication (iii) channel is busy because it is used by another device for transmission.
- Signal Energy detection: Energy detection request is created by MLME and issued to PLME. After detection of energy level it is reported back to MLME. The energy detection may fail due to unavailability of channel or due to a disabled radio.
- Enabling and disabling the radio transceiver: MLME may request the PLME to put the transceiver in one of the three states such as (i) transceiver disabled (ii) transmitter enabled (iii) receiver enabled.
- Obtaining information from PHY-PIB: MLME transmits requests to PLME for reading PHY attributes stored in PHY-PIB. After reading the values PLME provides it to MLME.

- Setting the value of PHY layer information base attribute: PHY layer can change the read-only PHY attributes and also all other attributes can be changed or set to a given value by receiving a request from MLME.

The work reported in this thesis is design of physical layer only.

2.3.6 MAC Services

The MAC layer acts as a interface between PHY and next higher layer to MAC such as network layer. The higher layer here is ZigBee networking protocol layer. Similar to PHY the MAC has also a sub layer reference model for its operation. Figure 2.4b describes this reference model clearly.

MAC sub layer can access the physical radio transceiver by a process of performing following tasks.

- Creates network beacon when the ZigBee device is a coordinator.
- Synchronization with network beacons
- Supports PAN association and disassociation
- Supporting the security of device
- Employs channel access mechanism such as CSMA-CA
- Maintains the Guaranteed Time Slot (GTS) mechanism
- Provides reliable link between two peer MAC layers.

MAC layer has two type of services namely Data service and management service. The MAC layer management entity (MLME) which performs management services accessed by MLME-SAP. It interacts with the counterpart of ZigBee network layer namely network layer management entity (NLME).The data service is accessed through MAC common part sub layer access points (MCPS-SAP). Like PHY, MAC has also its own data base known as

MAC PAN Information base (MAC-PIB), which includes all primitives and packet formats [1].

CSMA-CA

Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) is a channel access mechanism protocol without centralized control, which operates as follows [1]. Multiple devices can use the same frequency channel for their communication medium with the help of CSMA-CA.

The node that wants to transmit a data packet first performs the clear channel assessment procedure, i.e., it listens to the medium, for a prescribed time. If the medium is found to be free or clear (or idle) during that time, the node can transmit its packet. Otherwise if the channel is busy for transmitting another stations data or packet than the concerned station waits for a certain time for channel to be free. Different MAC algorithms used in different ways to calculate the time they need to listen to the channel during clear channel assessment procedure and to calculate the time to wait (i.e., the duration of the back off period) before the next transmission attempt. It is possible that the transmissions from two or more nodes overlap in time, which results in a collision and loss of all packets involved. If lossless communication is desired, collisions must be detected so that the lost packets can be retransmitted. Since a collision can be detected only at the receiver side, some form of acknowledgment from the receiver may be needed; some MAC protocols provide this facility, while others leave it to some of the upper layers like transport layer. In terms of reaction time, the MAC protocol facility is more efficient than the transport layer facility. In the basic CSMA protocol, carrier sensing is performed only at the sending node.

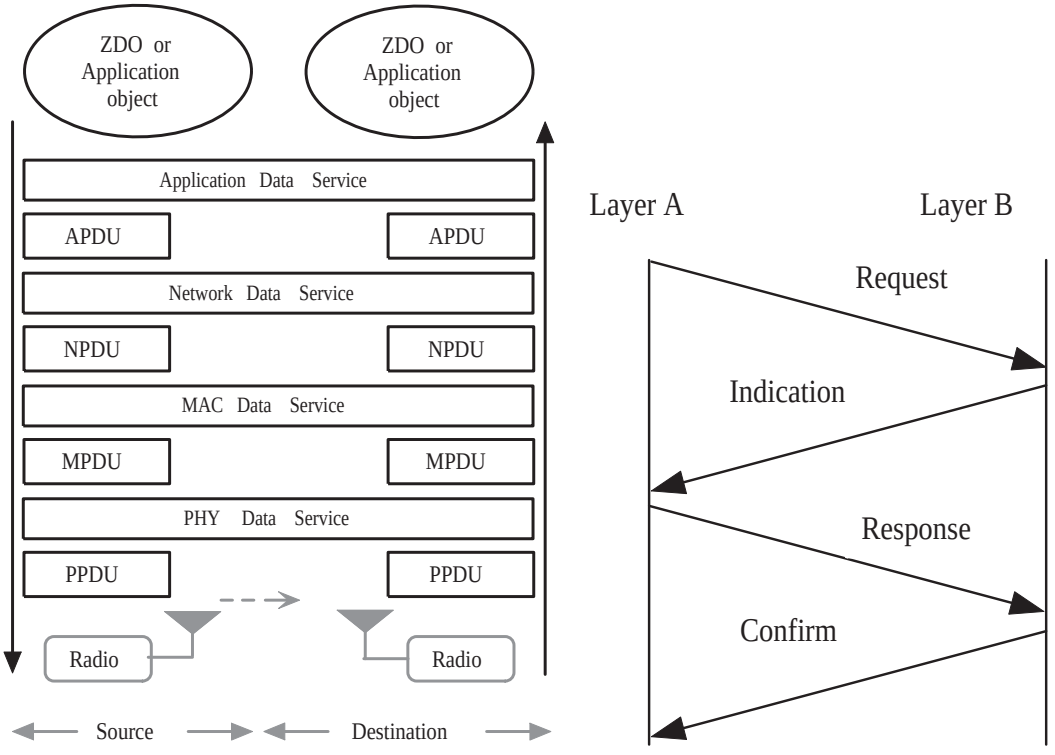
GTS

GTS stands for guaranteed time slot, which is helpful for network devices to transmit without using CSMA-CA. The PAN coordinator dedicates a specific time slot to a particular device. This is called a guaranteed time slot (GTS). Therefore, a device with an allocated

GTS will start transmitting during that GTS without using the CSMA-CA mechanism.

2.3.7 Data transfer between devices

When data is received by radio transceiver, the PHY layer notifies MAC layer for reception of MAC PDU (MPDU). PHY layer not only provides the MPDU to the MAC layer, it also delivers the Link Quality Indicator(LQI) information. Figure 2.5a presents the data transfer algorithm from application layer of one ZigBee device to another. The data always does not come from the application layer it may come from or generated by the MAC layer without involvement of upper layer. Data is provided by the ZigBee device object(ZDO) or an application object to application support sub layer (APS). During transmission data packet travels through all the layers and each layer adds its own header (preamble) with the data unit (DU) and then passes to the adjoining lower layer. Data unit in each layer is recognized by name of the layer and are defined as follows. [1].



(a) Data Transfer Between Layers (b) Two way Handshaking

FIGURE 2.5: Data Transfer Between Devices

- The data unit in APS layer is called application protocol data unit (APDU) after the addition of header and footer in APS layer.
- The data unit APDU received from APS is received by Network (NWK) layer and performs the header addition to produce the network protocol data unit(NPDU)
- Similarly the data unit in MAC layer is known as MAC protocol data unit(MPDU)
- The data unit (MPDU) from MAC layer received by PHY layer and reformed to PHY protocol data unit (PPDU) by adding the header which is later transmitted by radio.

on receiver side, the data unit is passed upward from lower layer to higher layer. The headers added in transmitter side are removed in different layers till data unit reaches the originated application layer.

2.3.8 Data Transfer Methods

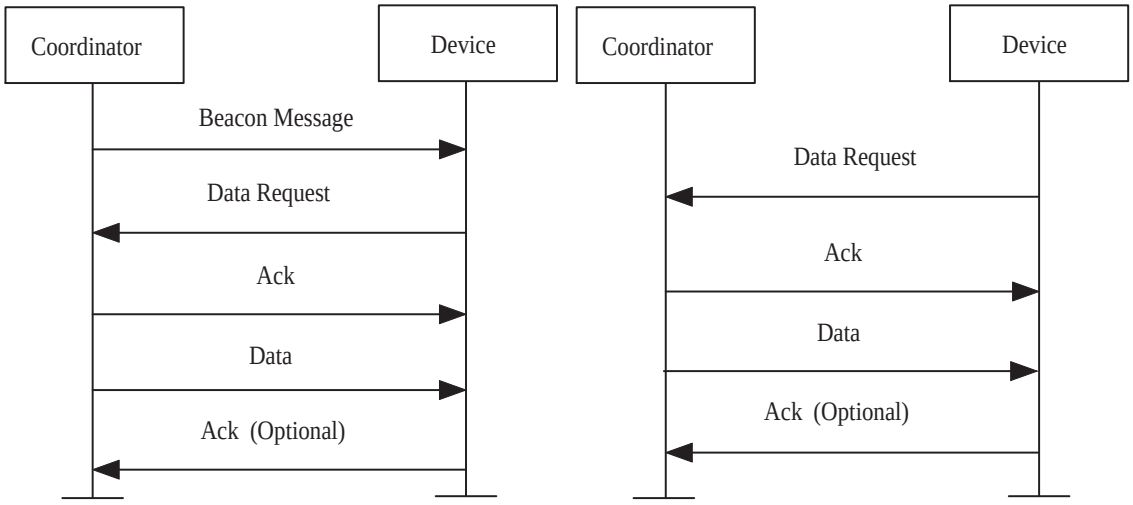
In the network the data packet travels through various nodes like network coordinator, end device, network router in the mesh networking topology[33][1]. Hence, to facilitate data communication the standard follows different types of data Transfer methods like.

- Data transfer from a device to a coordinator
- Data transfer from a coordinator to a device
- Data transfer between two peer devices

The data transfer in the network from device to coordinator or coordinator to a device can be classified as Beacon Enabled and Non-beacon Enabled, which are explained below.

- Beacon Enabled Data Transfer: In beacon enabled data transfer the PAN coordinator periodically transmits a beacon message. The PAN coordinator transmits beacon message to the devices associated with the network to ensure that all the devices are synchronized. The disadvantage of using beacon enabled data transfer is that all the

devices in the network wake up at regular intervals and listens to the beacon message for synchronizing their clocks and go back to sleep mode. In this case many devices in the network do not perform any other than clock synchronization [34]. This results higher power consumption comparison to non-beacon data transfer there by reducing battery life.



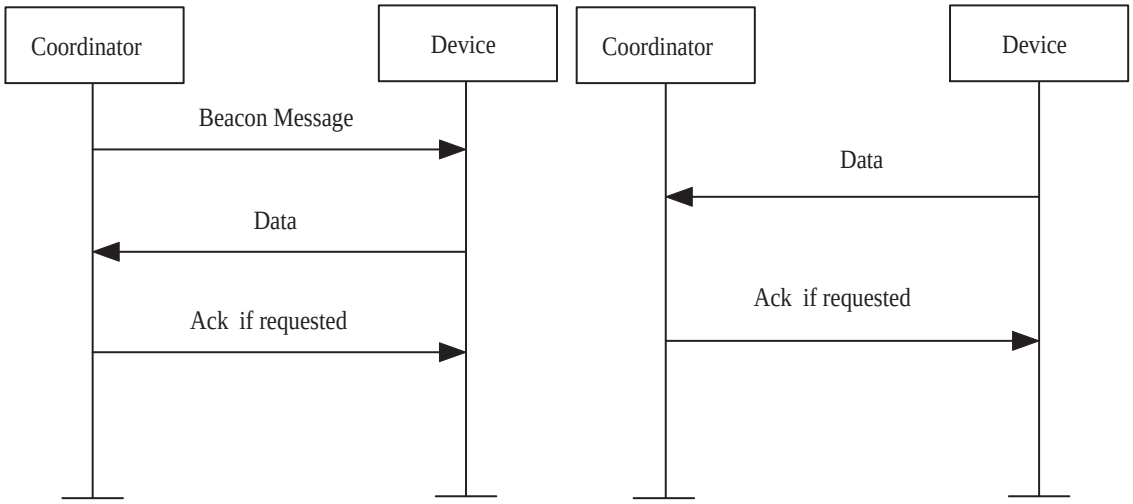
(a) Beacon Enabled (b) Non-beacon Enabled

FIGURE 2.6: Data Transfer From Coordinator to Network Device

- Non-Beacon Enabled Data Transfer: The ZigBee network where the PAN coordinator does not transmit beacon message is known as non-beacon network. In this case of data transfer, the devices in the network do not synchronize to each other which in turn consumes less power. Therefore the battery life is high in comparison to beacon enabled data transfer [35].

Data Transfer Primitive

Primitives convey the required information by providing a particular service. These primitives are an abstraction, because they specify only the provided service rather than the means by which it is provided. A service is specified by describing the service primitives and parameters that characterize it. A service may have one or more related primitives



(a) Beacon Enabled (b) Non-beacon Enabled

FIGURE 2.7: Data Transfer From Network Device to Coordinator

that constitute the activity which is related to the particular service. Each service primitive may have zero or more parameters used to convey the required information to provide the service.

The primitives can be of as follows

- Request: The request primitive is passed from layer A to layer B to request, that a service is initiated.
- Indication: The indication primitive is passed from layer B to layer A to indicate internal layer B event, that is significant to layer A. This event may be logically related to a remote service request or it may be caused by layer B internal event.
- Response: The response primitive is passed from layer A to layer B to complete the procedure invoked by indication primitive.
- Confirm: The confirm primitive is passed from layer B to layer A to convey the results of previous service requests

PHY layer management entity provides a set of service primitives for request and response which are described by 2.4 to 2.7. Communication between layer to layer takes

place through these service primitives.All primitives, PHY packet format (PPDU format) are processed as per the two way handshaking method as presented in Figure 2.5b.

$$< ThePrimitive > .request \tag{2.4}$$

$$< ThePrimitive > .indication \tag{2.5}$$

$$< ThePrimitive > .response \tag{2.6}$$

$$< ThePrimitive > .confirm \tag{2.7}$$

2.4 ZigBee 2.4 GHz PHY Specifications

The physical layer specification of ZigBee for 2.4 GHz frequency band supports 250 Kbps data rate with Modulation and spreading functions as described below.

2.4.1 Modulation and Spreading

2.4 GHz physical layer facilitates 16-ary quasi-orthogonal modulation technique. Each symbol transmitted consists of four information data bits which are used to select sixteen nearly orthogonal pseudo-random noise(PN) sequences. The PN sequences for all successive data symbols are concatenated during transmission. The aggregated chip sequence developed from DSSS are modulated on to carrier using offset quadrature phase-shift keying.

2.4.2 Reference Modulator

Figure 2.8 specifies the block diagram for modulation and spreading of physical layer for 2.4 GHz frequency band. The modulator and spreading functions including Bit to symbol mapping, Symbol to chip mapping and O-QPSK modulator are described as follows.

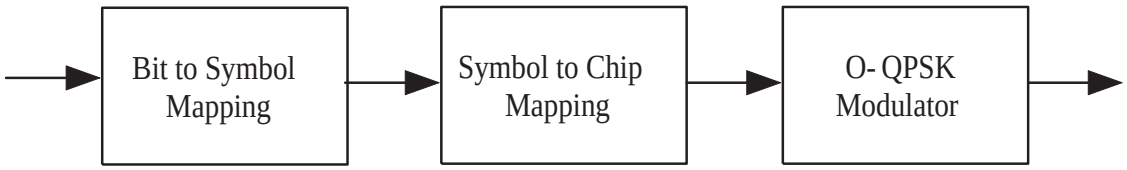


FIGURE 2.8: Modulation and spreading

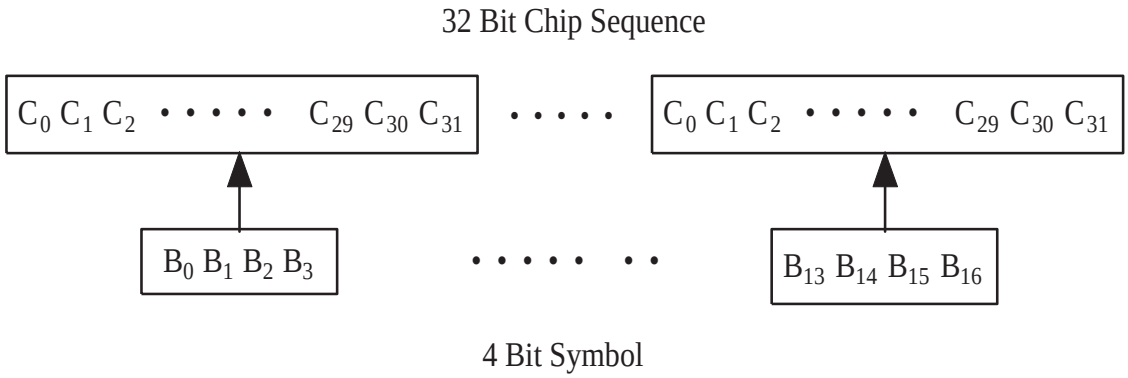


FIGURE 2.9: Symbol to chip mapping process

Bit to symbol mapping

Digital signal of data bit '1' and '0' inside the PHY Protocol Data Unit(PPDU) is encoded as per the spreading function. Here binary inputs are mapped to data symbols. For four bit symbol there are sixteen possible symbol starting from 0000 to 1111 are mapped to data symbol. Thus there are sixteen symbol to chip mapping as presented in following section.

Symbol-to-chip mapping

In this block each data symbol of 4 bits are mapped to 32 bit chip sequence as prescribed in the ZigBee standard. The process of mapping is presented in Figure 2.9 and the DSSS sequence for mapping is presented at Table 2.4 [36, 1].

Table 2.4: Symbol to Chip Mapping for 2.4 GHz Band

Data Symbol(Binary)	**Chip values** ($C_0\ C_1\ \ldots\ C_{31}$)
0000	11011001110000110101001000101110
1000	11101101100111000011010100100010
0100	00101110110110011100001101010010
1100	00100010111011011001110000110101
0010	01010010001011101101100111000011
1010	00110101001000101110110110011100
0110	11000011010100100010111011011001
1110	10011100001101010010001011101101
0001	10001100100101100000011101111011
1001	10111000110010010110000001110111
0101	01111011100011001001011000000111
1101	01110111101110001100100101100000
0011	00000111011110111000110010010110
1011	01100000011101111011100011001001
0111	10010110000001110111101110001100
1111	11001001011000000111011110111000

O-QPSK Modulation

Each data symbol is represented by 32 bit chip sequence which increases the chip rate by 32 times of symbol rate, and produces a 2 Mbps DSSS signal. Even bits and odd bits of DSSS signal is separated into I-phase data stream and Q-phase data stream by assigning odd bits and even bits as presented in Figure 2.10. To perform offset between I-phase and Q-phase data stream, the Q-phase chip is delayed by chip period(T_c) 2.10.

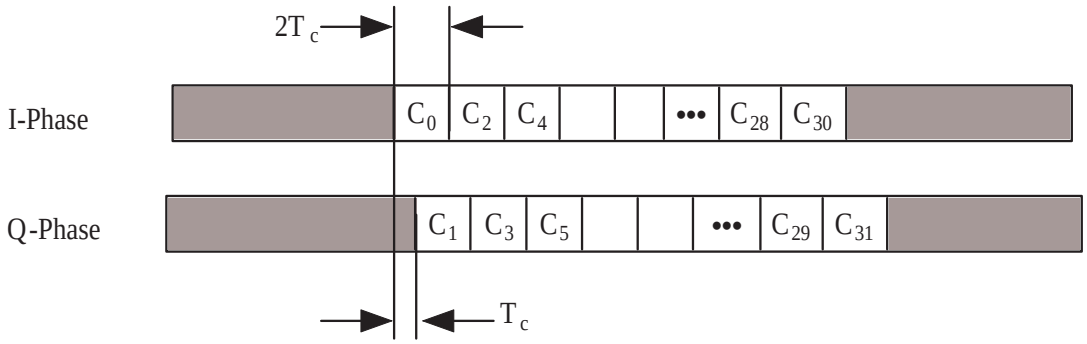


FIGURE 2.10: O-QPSK chip

Pulse shaping

Half sine pulse shaping of I-phase and Q-phase data stream is achieved by processing the signal with 2.8. This helps to reduce side lobes keeping inter symbol interference (ISI) low. The Pulse shaping process presented in Figure 2.11

$$p(t) = \begin{cases} \sin(\Pi \frac{t}{2T_c}) & 0 \leq t \leq 2T_c \\ 0 & otherwise \end{cases} \tag{2.8}$$

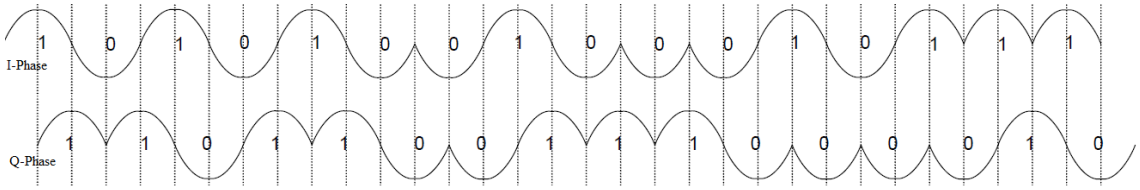


FIGURE 2.11: O-QPSK Pulshaping for I and Q Channel

2.5 Summary and Discussion

The analysis of ZigBee standard along with IEEE 802.15.4 standard for short range wireless communication explained briefly in this chapter. The analysis includes ZigBee networking topologies, various data transfer methods, ZigBee networking protocol layers and physical layer specifications for 2.4 GHz frequency band of IEEE 802.15.4 standard. The process of data transfer from between ZigBee devices with resource capability are presented in this chapter. During analysis it was found that ZigBee is one of the better technology of short range wireless applications like in industry automation, medical applications etc. Physical layer features such as input data rate, bit to symbol and spread spectrum for implementation of ZigBee baseband transceiver is analyzed here which is validated and implemented in next chapter.

3

FPGA Implementation of 2.4 GHz ZigBee Transceiver

In previous chapter, short range wireless communication for ZigBee was discussed. In order to develop the ZigBee transceiver the physical layer properties for 2.4 GHz described in previous chapter are taken as reference. This chapter presents the implementation process of ZigBee baseband transceiver. Which is simulated using hardware description language verilog HDL and finally implementation on VIRTEX 5 FPGA board.

3.1 ZigBee Transmitter in Simulink

With an aim for realization of ZigBee transceiver, the system was validated through MATLAB/Simulink environment in this section. The block diagram of ZigBee transmitter is presented in Figure 3.1. This transmitter design in Simulink is shown in Figure 3.2 which is explained in following subsections.

IEEE 802.15.4 standard uses the spreading methods to improve the effect of receiver sensitivity, jamming resistance, and also to reduce the effect of multi path interference [37, 38]. The spreading technique used here is DSSS. In this, every four incoming data bit is combined together to form a four bit symbol and this four bit symbol is mapped onto an unique 32 chip sequence available in a lookup table. Hence there are sixteen different 32 bit chip sequences. The set of chip sequences is shown in Table 2.4. The chip sequences

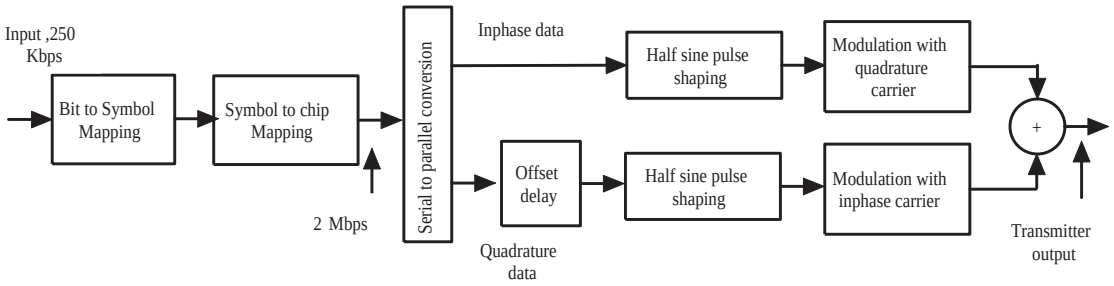


FIGURE 3.1: Block Diagram of ZigBee transmitter

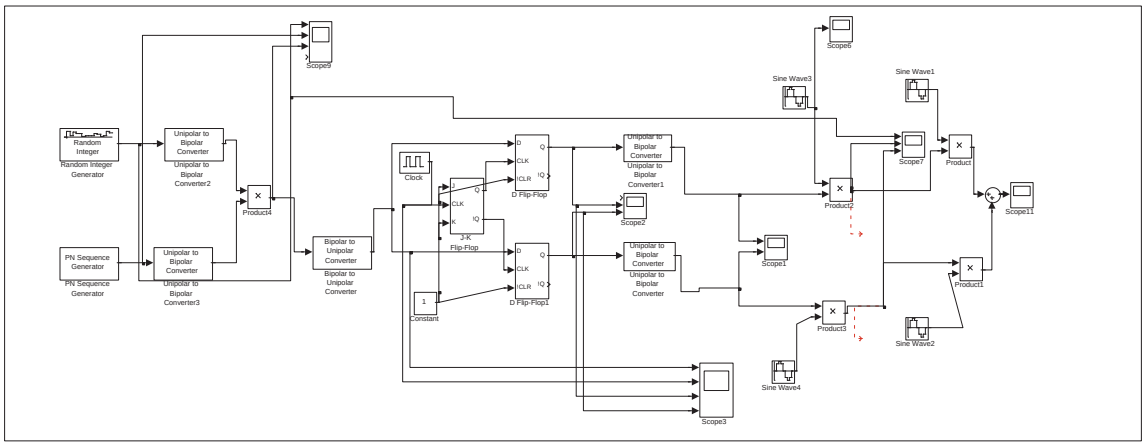


FIGURE 3.2: Simulink Model of ZigBee Transmitter

are also known as Pseudo random noise sequence (PN sequence). The chip sequence is the collection of zeros and ones. To avoid the similarity between any two chip sequences, the standard follows a procedure or algorithm of doing the cross-correlation between the chip sequences. The cross-correlation is calculated by multiplying the sequences together and then calculating the summation of the result. The 32 bit chip sequence contains a sequence of zeros and ones in unipolar form. Before calculation of the cross correlation the unipolar sequence is converted to bipolar sequence ie a '0' is represented by '-1' and '1' is as it is. If x(n) and y(n) are two sequences then the cross correlation of x(n) and y(n) is calculated by 3.1.

$$r_{xy}(0) = \sum_{n=-\infty}^{n=\infty} x(n)y(n) \tag{3.1}$$

The relation 3.1 and 3.2 calculates the cross correlation of x(n) and y(n) where neither of these sequences shifted. Hence it defines that the two sequences are dissimilar to each other. In this case the sequences are known as orthogonal to each other and termed as orthogonal sequences. The sixteen pseudo noise sequences used in the standard IEEE 802.15.4 are not completely orthogonal to each other and are called as quasi orthogonal or nearly orthogonal [2]. The cross correlation of other Pseudo Noise(PN) sequences are calculated by shifting one sequence with a margin of time period 'k' hence the relationship is presented as 3.2

$$r_{xy}(k) = \sum_{n=-\infty}^{n=\infty} x(n)y(n-k) \tag{3.2}$$

3.1.1 Symbol to Chip Mapping

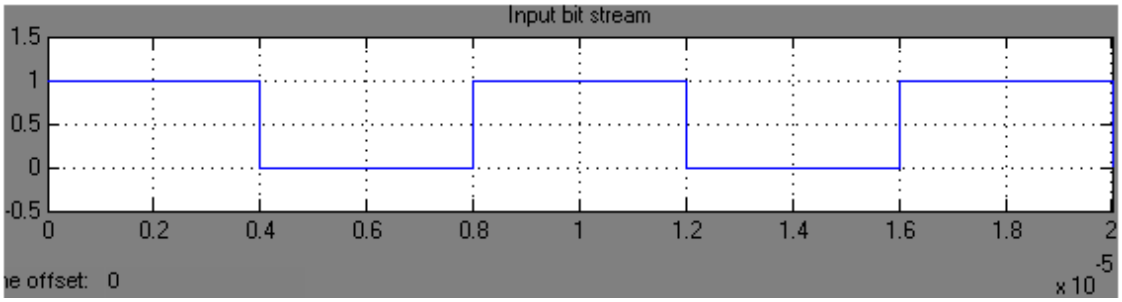
ZigBee can transmit data at 250 Kbps.

- A input data stream of 250 Kbps was generated by using random integer generator block in communication tool box. The parameters like M- ary number, initial seed, sample time and output data type are configured to get fixed binary stream. In a real time scenario, this data stream is supplied by application that will generate information to be transmitted [11].

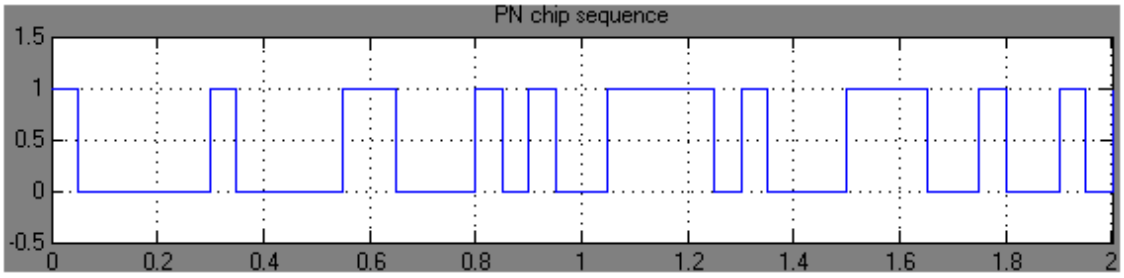
- Using PN sequence generator block in communication tool box, the 32 bit PN sequence is generated from 4 bit symbol. This sequence is of 2 Mbps. The parameters for generator polynomial, initial states, sample time and output data type were adjusted to generate the 32 bit Pseudo Noise code.

- The input data stream and PN code are converted to Non Return to Zero (NRZ) format and multiplied to each other to generate DSSS signal.

An input data stream, a PN sequence and DSSS output for a ZigBee transmitter generated using Simulink is presented in Figure 3.3a, 3.3b and 3.4.



(a) Input data in Simulink



(b) pnsequence

FIGURE 3.3: Input data and PN sequence

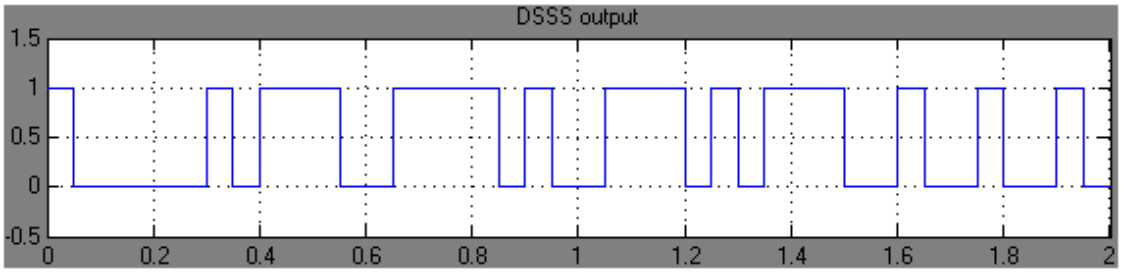


FIGURE 3.4: DSSS output in Simulink

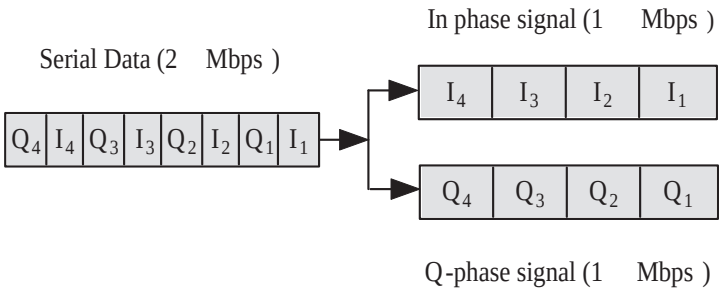


FIGURE 3.5: Serial to Parallel Conversion

3.1.2 Serial to Parallel Conversion

ZigBee standard uses OQPSK modulation. In order to achieve this. the input chip sequence of 2 Mbps serial data stream is converted to even bit stream and odd bit stream by splitting the sequence to even bit and odd bit of serial data stream separately. This is presented Figure 3.5. From the figure it is clear that the odd bits are assigned to odd bit stream and even bits are assigned to even bit stream by naming the signal as I-phase signal and Q-phase signal respectively.

with the help of Simulink tool box, the I-phase and Q-phase signal extracted from the DSSS serial data, each of these is 1 Mbps. Splitting the signal into I-phase and Q-phase requires a clock, a JK flip flop and two D flipflops. Aligning the odd and even streams in time requires half bit offset which is achieved with D flip flop. The I-phase signal and Q-phase signal after serial to parallel conversion taken from the simulink scope is given in Figure 3.6a and 3.6b respectively.

3.1.3 Half sine pulse shaping

The NRZ form of I-phase and Q-phase data of shape sharp edges. Transmission of these would generate large number of side bands. In order to remove side bands the pulses to be transmitted and passed through a pulse shaping circuit. This is achieved by multiplying the signal with 90° out of phase sine waves to get the half sine pulse shaping. This is shown in Figure 3.12a and 3.12b.

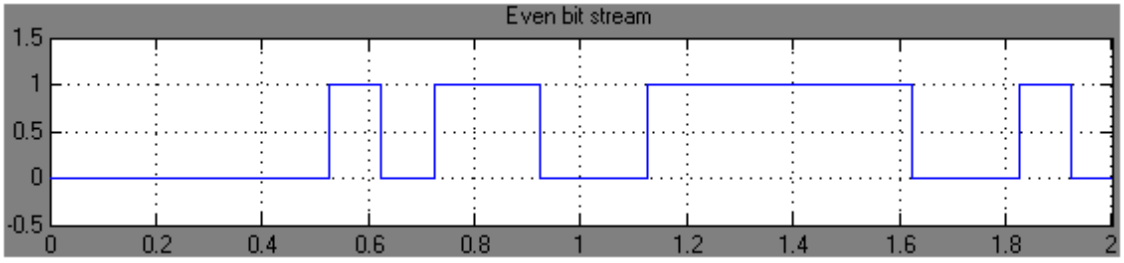
3.1.4 RF Modulation

After pulse shaping the even bit stream $b_e(t)$ is superimposed on a carrier $\sqrt{2p_s}\cos\omega_0 t$ and the odd bit stream $b_0(t)$ is superimposed on a carrier $\sqrt{2p_s}\sin\omega_0 t$ with the use of two multipliers. This generates two signals, these are $s_o(t)$ and $s_e(t)$ respectively. These signals are then added to generate transmitted output signal $v_m(t)$ which is given by (3.3).

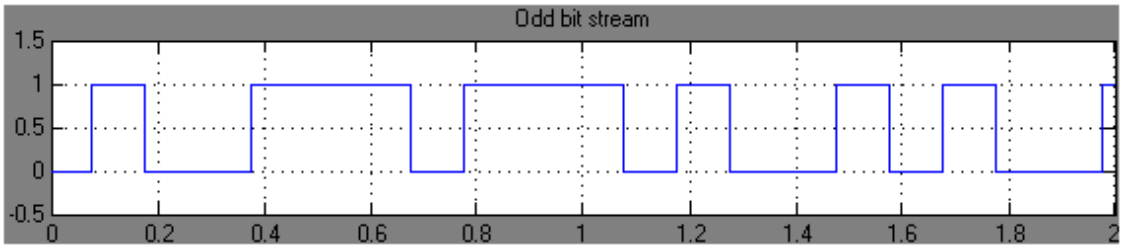
$$v_m(t) = \sqrt{2p_s}s_o(t)\cos\omega_0 t + \sqrt{2p_s}s_e\sin\omega_0 t \tag{3.3}$$

The two terms in (3.3) represents the I-phase stream $s_o(t)$ and Q-phase stream $s_e(t)$. Both $s_e(t)$ and $s_0(t)$ occupy the same spectral range but they are individually identifiable because of the phase quadrature of the carriers. These four possible output signals have equal amplitude $\sqrt{2p_s}$ and are in phase quadrature. They have been identified by their corresponding values of b_0 and b_e.

This modulation is carried out with 2.4 GHz high frequency sinusoidal carrier. By using sine wave block in Signal Processing tool box, 2.4 GHz high frequency signal is



(a) I-phase data in Simulink



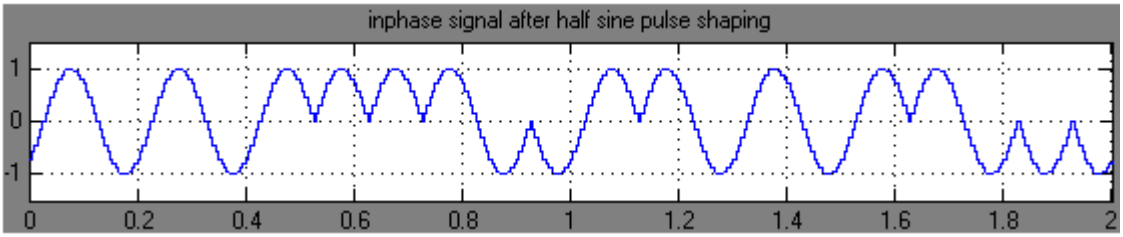
(b) Q-phase data in Simulink

FIGURE 3.6: Serial to Parallel conversion in Simulink

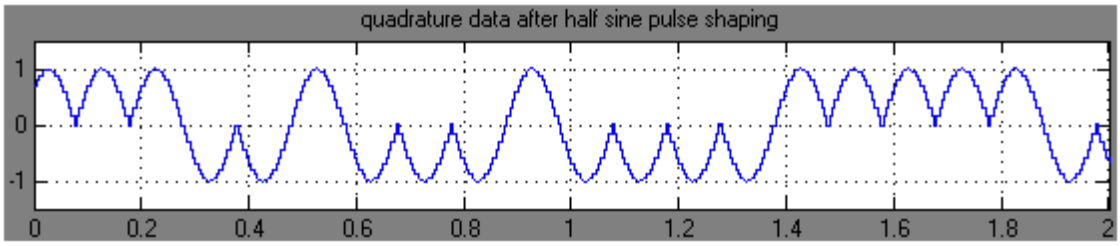
generated by adjusting signal processing tool box parameters. Then I-phase half sine pulse shaping signal is multiplied by a sine wave and Quadrature half sine pulse shaping signal is multiplied by its orthogonal carrier i.e., cosine signal which is 90° phase shift of original sinusoidal carrier. After modulation the I-phase and Q-phase signal outputs taken from Simulink scope is presented in Figure 3.8a and 3.8b. Then signals are combined together to get the transmitter output in 'sum' block from commonly used blocks as obtained in Figure 3.8c

3.2 ZigBee Receiver in Simulink

This section describes ZigBee receiver architecture and its validation in Simulink. The block diagram of ZigBee receiver and simulink design is presented in Figure 3.9 and 3.10 , here coherent detection has been used. The receiver implements reverse process of transmitter blocks and consists of demodulation, halfsine pulse shaping, low pass filter, sample and hold, comparator and despreading. following sub sections describes each of the blocks.



(a) I-phase pulse shaping in Simulink



(b) Q-phase pulse shaping in Simulink

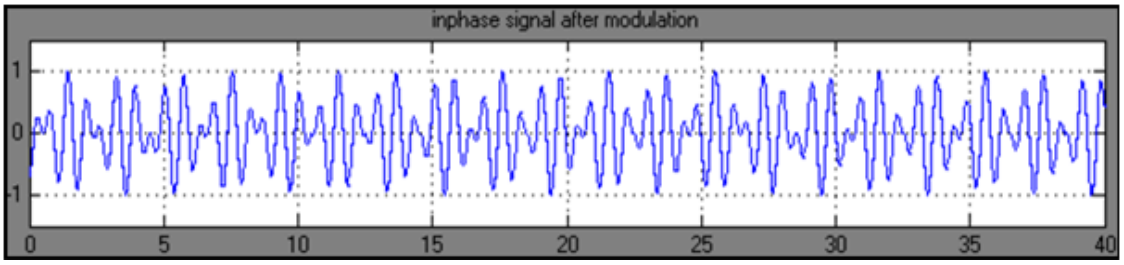
FIGURE 3.7: I-phase and Q-phase pulse shaping in Simulink

3.2.1 Receiver Operation

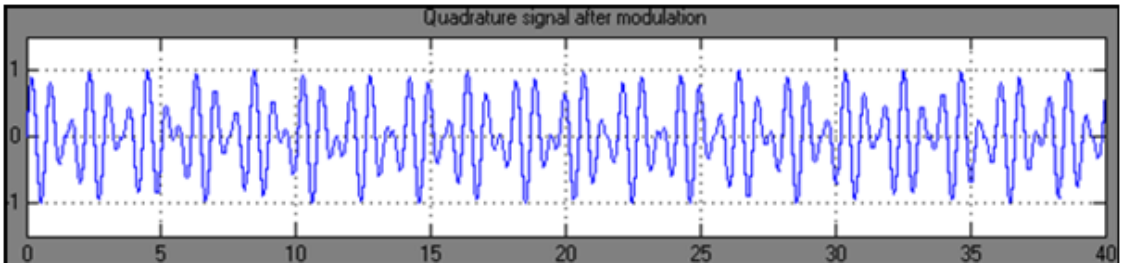
The incoming received signal is applied to two synchronous demodulators, each of which consists of amultiplier followed by a low pass filter. The received signal signal from two modulators are 90° out of phase. They can be represented as 3.4 and 3.5.

$$c_1 = \cos(\omega_0 t)\cos 2\Pi\frac{t}{4T_b} + n(t) \tag{3.4}$$

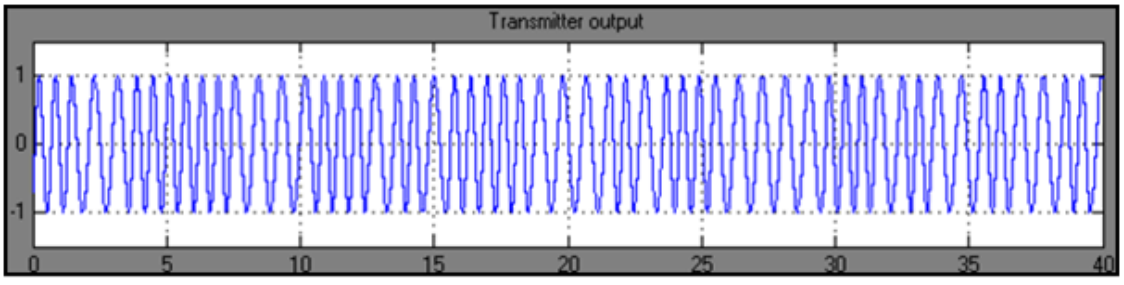
$$c_2 = \sin(\omega_0 t)\sin(2\Pi\frac{t}{4T_b}) + n(t) \tag{3.5}$$



(a) I-phase modulation signal through Simulink



(b) Q-phase modulation signal through Simulink



(c) transmitter output at Simulink

FIGURE 3.8: Modulation output waveform

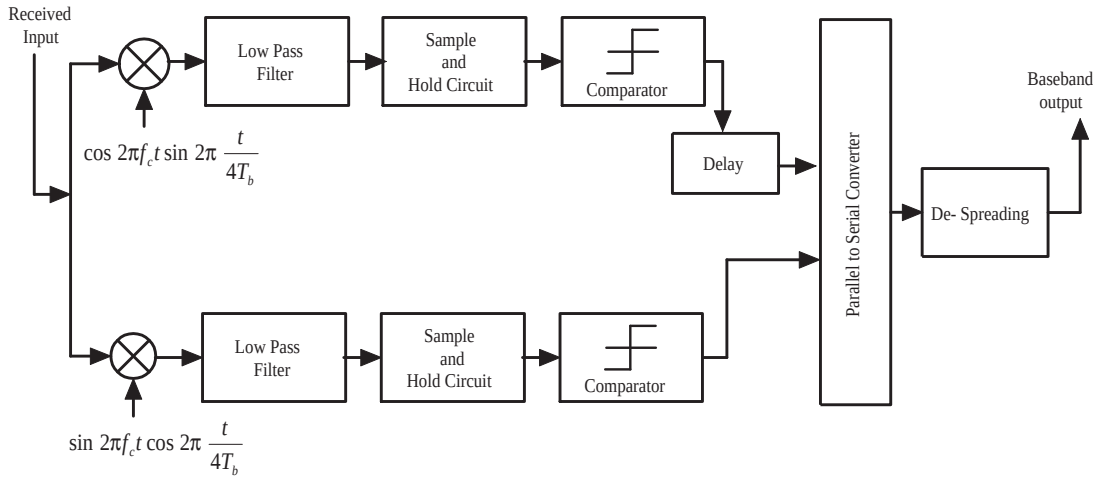


FIGURE 3.9: Block Diagram of ZigBee Receiver

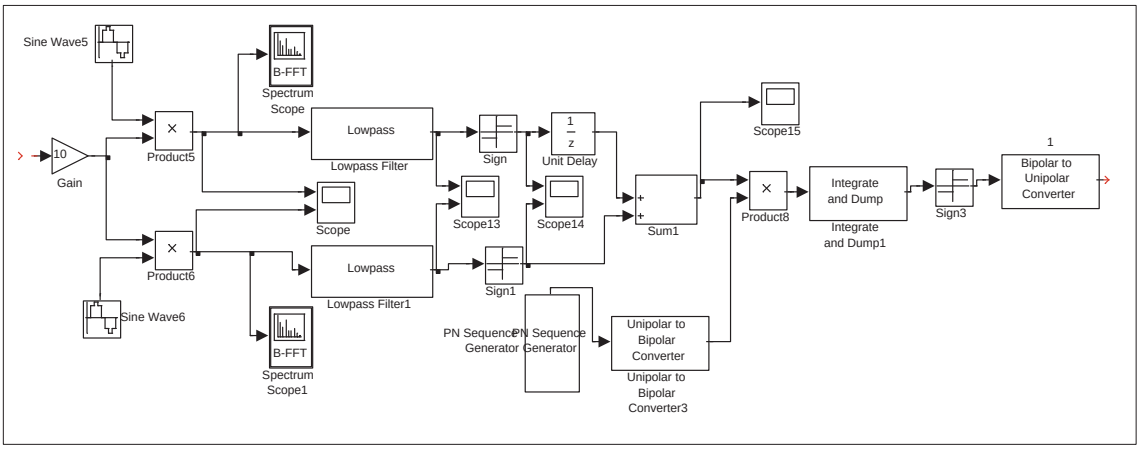


FIGURE 3.10: Simulink Model of ZigBee Receiver

Where, c_1 and c_2 are transmitted signal and $n(t)$ is AWGN. Here it has been assumed that the channel is single path AWGN channel.

The demodulator at receiver is a coherent receiver its output contains baseband data and higher frequency harmonics represented as (3.4) and (3.5). Higher frequency harmonics are removed from the signal by passing through a low pass filter. Generally, a third order Butterworth filter having a cutoff frequency of $2/T_b$ Hz is used for the extraction of baseband data. The resultant signal after low pass filter is passed through a zero order sample and hold circuit which holds the data for one bit period, later is passed through a decision device comparator for thresholding. For signal data levels s_1 and s_2 the threshold is provided by (3.6), if input to comparator is greater than threshold value, it decodes the bit as '1' otherwise it decodes as '0'.

$$s^*(t) = \frac{s_1 + s_2}{2} \tag{3.6}$$

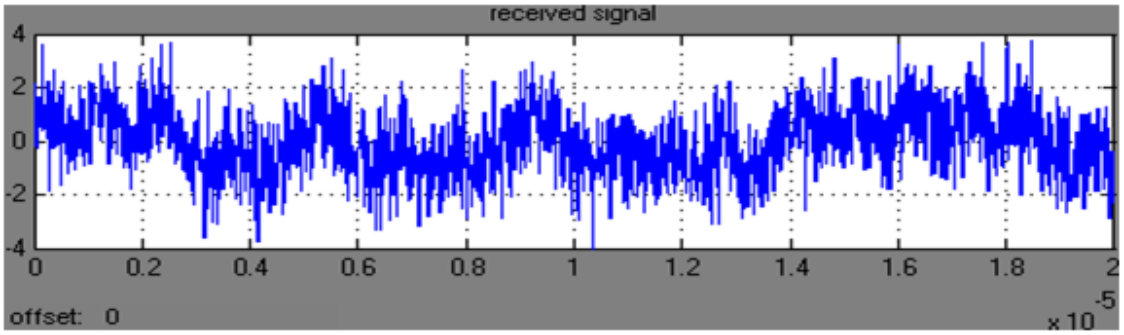
3.2.2 Demodulator

In the process of FPGA design of ZigBee receiver, the performance of ZigBee receiver was first analyzed in simulink environment. The performance of simulation using Simulink is presented below.

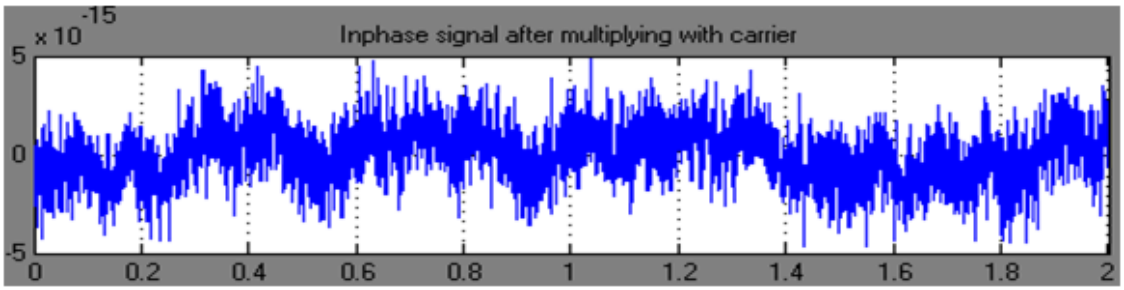
The performance ZigBee receiver was corrupted with AWGN and the noisy signal is considered as received signal. This signal was at 2.4 GHz carrier frequency. This noisy received signal is presented in Figure 3.11a is passed through I-phase and Q-phase demodulator for 2.4 GHz carrier frequency and 90° phase shift between them. The demodulated I-phase Q-phase signal are displayed in Figure 3.11b and 3.11c respectively.

3.2.3 Half sine pulse shape

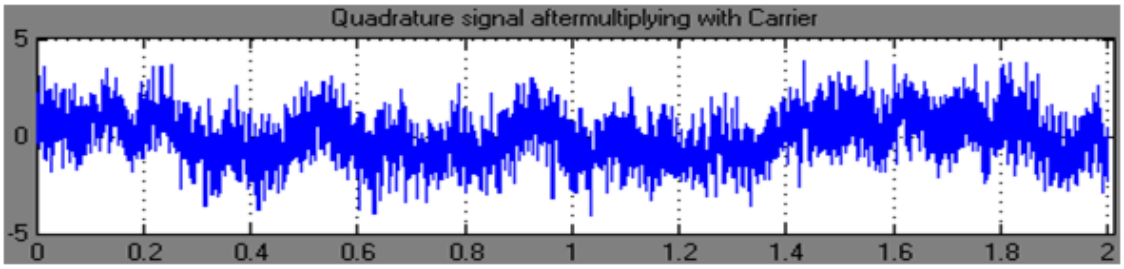
In OQPSK, abrupt phase changes occurs due to the multiplication of abrupt rectangular baseband waveform with the Quadrature carrier causing loss of phase continuity, so there is no phase continuity. These abrupt changes give rise to spectral components at high



(a) Received signal with noise in Simulink



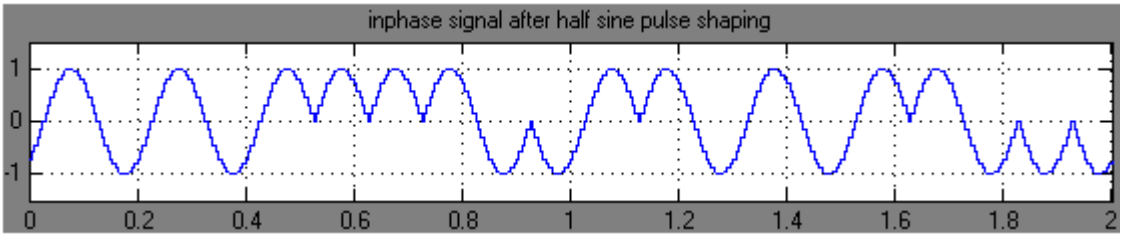
(b) I-phase demodulation in Simulink



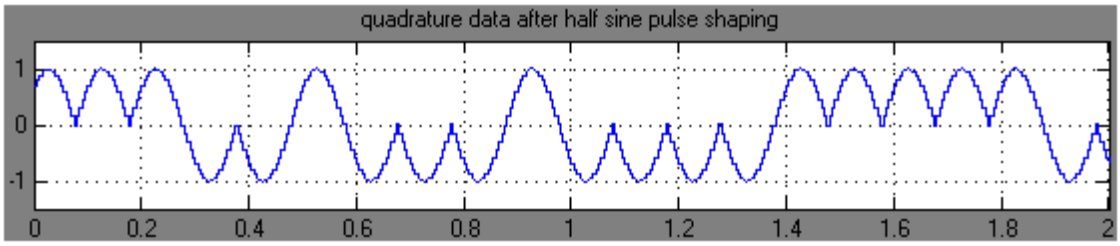
(c) Q-phase demodulation in Simulink

FIGURE 3.11: Demodulation in Simulink

frequencies. The baseband spectral range is very large and multiplication by a carrier translates the spectral pattern without changing its form. It is required to alleviate this difficulty by passing the baseband signal through a low pass filter to suppress the side lobes. Such filtering cause inter symbol interference. To overcome this problem half sine pulse shaping can be implemented. In this design, half sine was used for pulse shaping to exhibit phase continuity and to smoothen the baseband waveform. This is achieved by multiplying sine wave with a the bit period of $4T_b$ in both I and& Q channel.



(a) I-phase pulse shaping in Simulink



(b) Q-phase pulse shaping in Simulink

FIGURE 3.12: I-phase and Q-phase pulse shaping in Simulink

3.2.4 Low Pass Filter

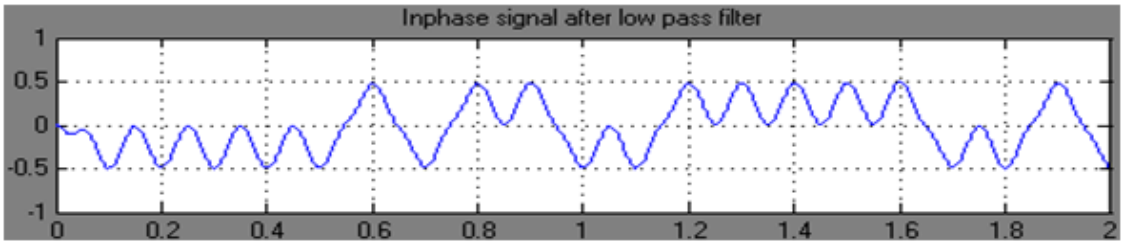
A low pass filter of cutoff frequency 500 KHz is designed by using analog filter design block, where the parameters like design method, filter type, filter order and pass band edge frequency are configured. The output of low pass filter in both I-phase and Q-phase is presented in Figure 3.13a and 3.13b. The two outputs are next fed to sample and hold circuit.

3.2.5 Sample and Hold

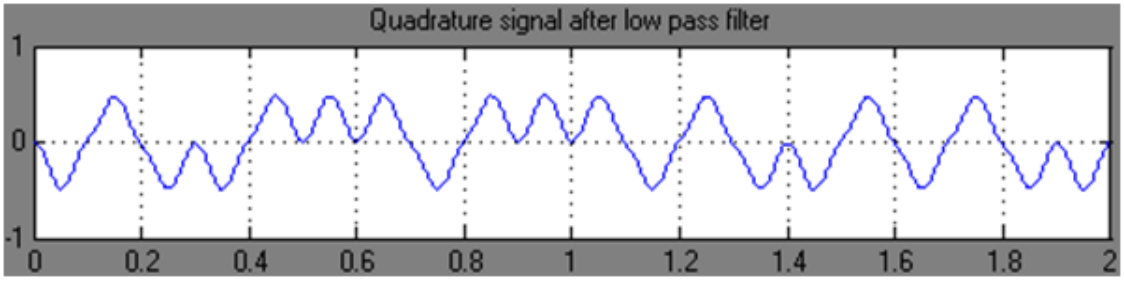
The sample and hold circuit samples the signal for every T time period, by using sample time and time period T in zero order hold circuit. Here a relative time period of $2\mu s$ is used for sampling to get the sample and hold output as shown in Figure 3.14a, 3.14b. The output taken from this stage forms the even and odd bit stream from receiver.

3.2.6 Parallel to serial conversion

The I-phase signal and Q-phase signal at receiver combined together in a switch block to form the 2 Mbps serial data, which is the DSSS signal transmitted by the transmitter. To make accurate alignment between I-phase and Q-phase during combination, a half bit delay is introduced to I-phase signal at receiver. Here the parameters like threshold value and criterion for parallel to serial conversion is optimized to generate 2 Mbps serial data as shown in Figure 3.16a.

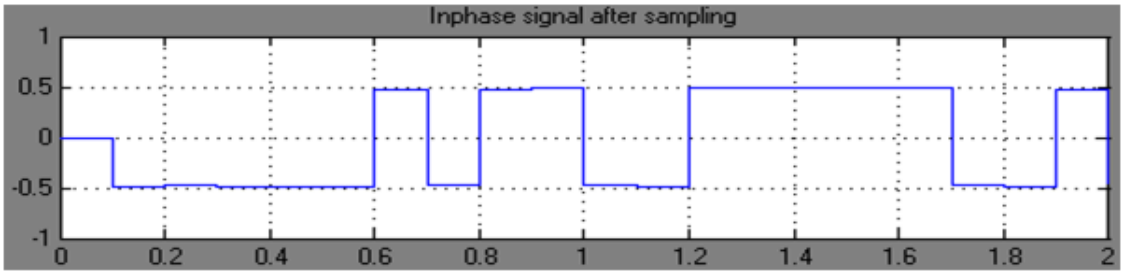


(a) I-phase through low pass filter

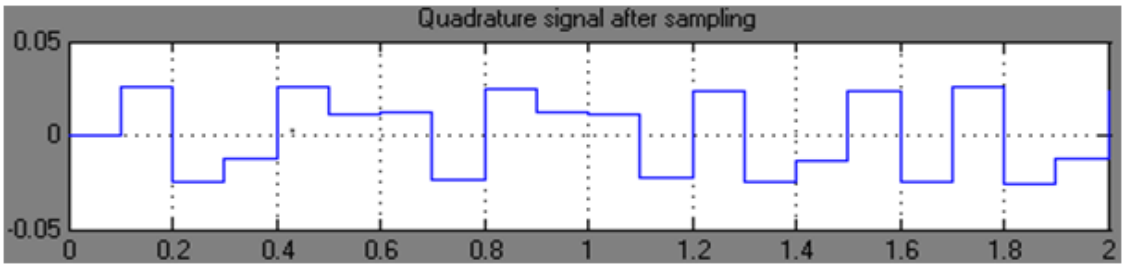


(b) Q-phase through low pass filter

FIGURE 3.13: I-phase and Q-phase passed through low pass filter

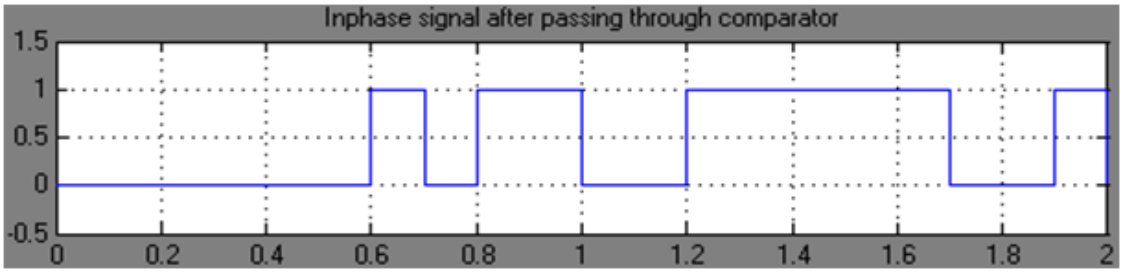


(a) I-phase after sampling

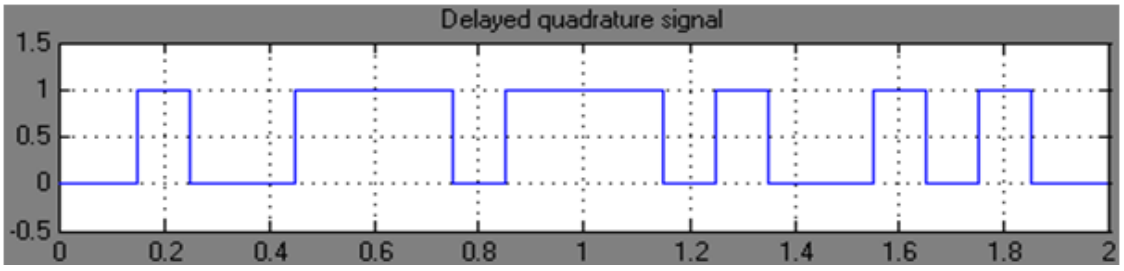


(b) Q-phase after sampling

FIGURE 3.14: I-phase and Q-phase passed through sampled and hold



(a) I-phase data stream at receiver

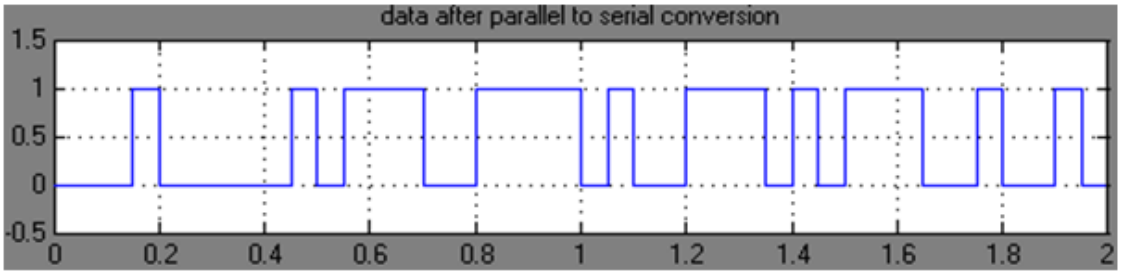


(b) Q-phase data stream at receiver

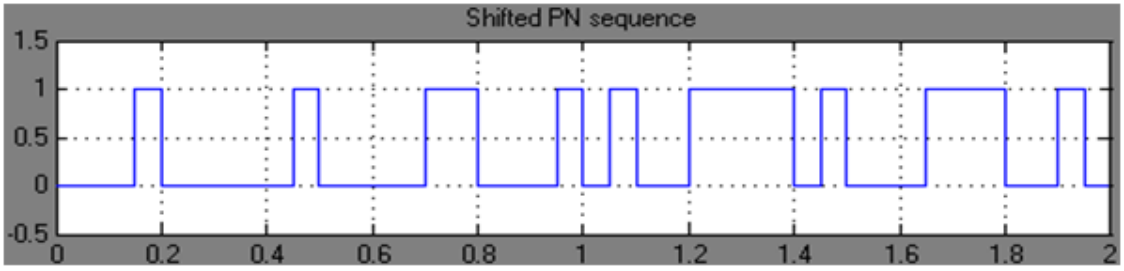
FIGURE 3.15: I-phase and Q-phase passed through comparator

3.2.7 Despreading

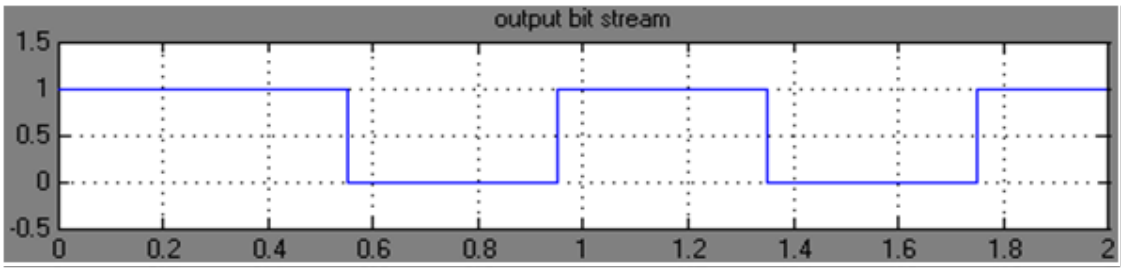
The received 2 Mbps DSSS signal is despreaded by using same PN sequence which is used for serial to parallel conversion at transmitter. The original data stream is received by multiplying the PN sequence with DSSS signal which is presented at Figure 3.16a. Here the PN sequence is the replica of PN sequence used in transmitter.



(a) 2 Mbps serial data stream at receiver



(b) PN sequence at receiver



(c) Baseband output data

FIGURE 3.16: Despreading at receiver

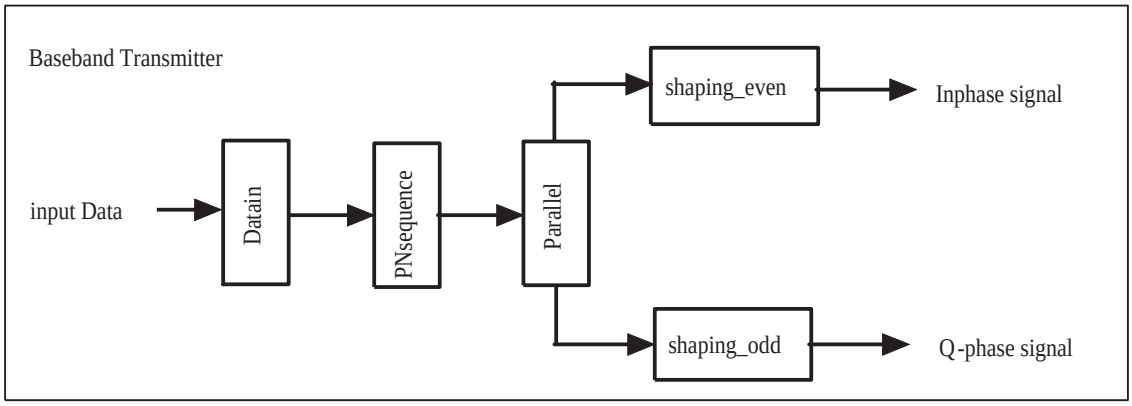


FIGURE 3.17: ZigBee baseband Transmitter

3.3 Baseband Transmitter Design for FPGA

Following the simulation of ZigBee transceiver in simulink, the transceiver was described in verilog HDL and simulated on modelsim before downloading the design to FPGA. After the transmitter was thoroughly simulated in MATLAB/Simulink, the transmitter was designed using hardware description language verilog HDL and implemented in FPGA as per the reference modulator diagram mentioned in Chapter 2 [1]. The basic baseband module of ZigBee transmitter for implementing in FPGA presented in Figure 3.17. The transmitter consists of following stages.

3.3.1 Input data stream

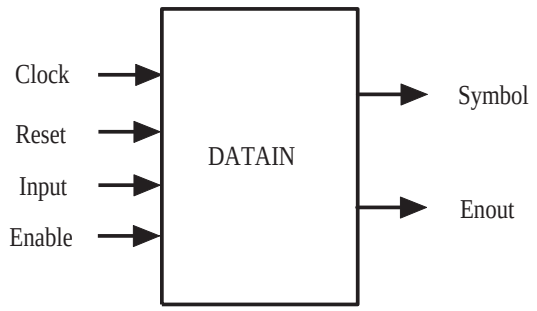
Input data stream is a sequence of binary bits which is the input signal to transmitter. The input data is stored in a memory and read from the memory. The input data bit is transmitted at a rate of 250kbps. So in the design at every $4\mu s$ one binary input bit is transmitted. Clock signal of $4\mu s$ time period is generated by the Digital Clock Manager(DCM). The design of clock circuit is presented in FPGA implementation section, it provides clock signal for 10 MHz, 1 MHz, 250 KHz.

Table 3.1: I/O Description Datain Module

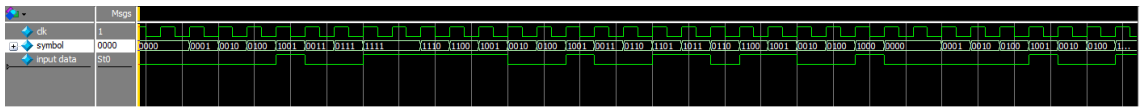
SL No	PIN Name	Direction	Size	Description
1	Clock(clk)	Input	1	Synchronous Clock of 250 KHz
2	Reset	Input	1	Asynchronous Reset
3	Input	Input	1	Data input
4	Enable	Input	1	Valid Signal for input Data
5	Symbol	Output	4	4 bit output termed as symbol which is of data rate 62.5 kilo symbol per second
6	Enout	output	1	Valid Signal for output Data

Input Output Description of Datain Module

The first block of transmitter is the input data to symbol conversion. In verilog HDl design the incoming data bits 1 and 0 are stored in a 4 bit register to form a symbol, which is having 62.5 kilo symbols per second. Input output diagram of input module is depicted in Figure 3.18a and Table 3.1 presents its description. The signals shown in Figure 3.18b represents clock signal of frequency 250 KHz named as 'clk', the incoming data bit consisting of four bit symbol named as 'symbol' and one bit input data of 250 Kbps named as 'input data' for 270000 ns simulation time.



(a) I/O Diagram of Datain Module



(b) Bit to symbol Mapping(Modelsim Simulation)

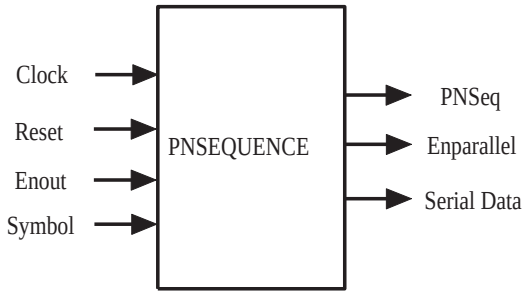
FIGURE 3.18: Bit to Symbol

3.3.2 Symbol to chip conversion

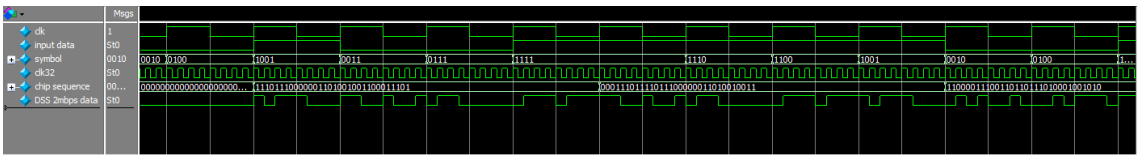
As per ZigBee baseband design at 2.4 GHz, a combination of 4 bit input data symbol provide the respective 32 bit chip sequence for IEEE 802.15.4, this was presented in Table 2.4. Symbol to chip mapping produces a 2 Mbps serial unipolar signal which is performed OQPSK modulation in parallel to serial block. In HDL design, 32 bit chip sequence are transmitted by clock signal 'clk' generated by DCM.

Input Output Description

Input to this module is 4 bit symbol, which are mapped to 32 bit chip sequence resulting a output of 2 Mbps serial data. The I/O description of this module is presented in Table 3.2 . The signal output for this subsystem is presented at Figure 3.19b. Figure 3.19b displays clock signal of frequency 250 KHz named as 'clk', the incoming input data of 250 Kbps named as 'input data', data symbol consists four input data bit named as 'symbol', clock signal of frequency 1 MHz named as 'clk32', 32 bit chip sequence in 32 bit register inside the PNSEQUENCE module named as 'chip sequence' and 2 Mbps direct sequence spread spectrum signal named as 'DSSS 2 mbps data' for 270000 ns simulation time.



(a) I/O Diagram of PNSEQUENCE Module



(b) Symbol to chip Generator(Modelsim Simulation)

FIGURE 3.19: Symbol to chip and DSSS

Table 3.2: I/O Description pnsequence module

SL No	PIN Name	Direction	Size	Description
1	Clock(clk32)	Input	1	Synchronous Clock of 1 MHz
2	Reset	Input	1	Asynchronous Reset
3	Enout	Input	1	Valid Signal for input Data
4	Symbol	Input	4	4 bit input termed as symbol which is of data rate 62.5 kilo symbol per second
5	PNSeq	Output	1	2 Mbps output after symbol to chip mapping
6	Enparallel	Output	1	Valid signal for output data
7	Serial Data	Output	1	2 Mbps DSSS output after spread spectrum

3.3.3 Serial to Parallel Conversion

After Symbol to chip mapping serial data constitute a 2 Mbps digital signal which is the combination of all chip sequences as per the symbol at input. ZigBee standard at 2.4 GHz uses OQPSK modulation. For this reason the DSSS serial data is converted to a 2 channel parallel data for I and Q processing channels. Serial to parallel conversion is implemented with a set of flip flops and flag registers in verilog HDL design.

In verilog HDL design the serial to parallel conversion is performed with the help of Digital Clock Manager(DCM) clock signal clk32 of 1 MHz. During the active edge of clock period along with the the flag value 2 Mbps serial data converted to two 1 Mbps parallel data. during conversion the odd bits of serial data assigned to oddbit stream and even bits are assigned to even bit stream. since the first bit of the serial data is an odd bit it is assigned first and even bit assigned next. the process continues as long as input serial data is available.

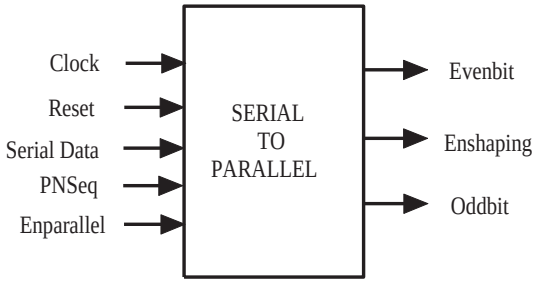
Input Output Description

After chip mapping the output is 2 Mbps serial data in pnsequence module, which is separated in to I-phase signal and Q-phase signal in this module. I-phase signal contains the odd bits and Q-phase signal contains even bits of serial 2 Mbps signal. I/O description of this module is presented in Table 3.3. The modelsim result from simulation is presented

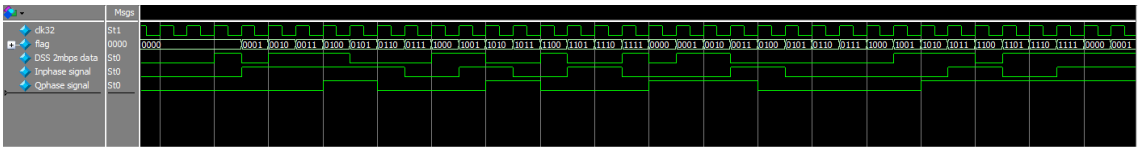
Table 3.3: I/O Description of Serial to Parallel

SL No	PIN Name	Direction	Size	Description
1	Clock(clk32)	input	1	Synchronous Clock of 1 MHz
2	Reset	input	1	Asynchronous Reset
3	Enparallel	input	1	Valid Signal for input Data
4	Serial Data	input	1	After DSSS the 2Mbps data stream
5	PNSeq	input	1	chip sequence without spread spectrum
6	Enshaping	output	1	Valid Signal for pulse shaping
7	Oddbit	output	1	Every oddbit of serial data stream assigned to this pin
8	Evenbit	output	1	Every Evenbit of serial data stream assigned to this pin

at Figure 3.20b for 270000 ns simulation time. This figure includes the clock signal 'clk32' of frequency 1 MHz, 32 bit register named as 'flag' consists of 32 bit chip sequence, spread spectrum signal of 2 Mbps data rate named as 'DSSS 2 Mbps data', I-phase signal and Q-phase signal named as 'Inphase signal' and 'Qphase signal' respectively. Each of these signals becomes 1 Mbps data rate after serial to parallel conversion.



(a) I/O Diagram of Serial to parallel Converter



(b) Serial to parallel(Modelsim Simulation)

FIGURE 3.20: I-phase Q-phase separation

Table 3.4: Samples for Pulse shaping

Sampling time (ns)	Sample value for bit 1	Sample value for bit 0 in twos complement
100	00000000	00000000
200	00010000	11110000
300	00100000	11100000
400	00110000	11010000
500	00111000	11001000
600	01000000	11000000
700	00111000	11001000
800	00110000	11010000
900	00100000	11100000
1000	00010000	11110000

3.3.4 ZigBee transmitter Pulse Shaping

In our design unipolar signal has been used. Here during symbol to chip conversion the verilog logic replaces '-1' with '0' and '1' is left as it is. During Pulse shaping the bits one and zero in even stream and odd stream are shaped by half sine wave, hence the name is half sine pulse shaping. Here pulse shaping has been implemented by taking continuous values from lookup table in memory. Here stored sample values are multiplied with respect to bit one and zero of even bitstream and odd bitstream to generate continuous value signals.

The samples are multiplied with the help of flag value and DCM. The even bitstream and odd bit stream are of time period 1000 ns. So for every 100 ns one sample is multiplied as per the flag value to get the pulse shape as shown in simulation result presented in Figure 3.21b and 3.22b. The lookup table uses 10 continuous values for pulse shaping. More samples can be multiplied to get the sharpness in the pulse shaping.

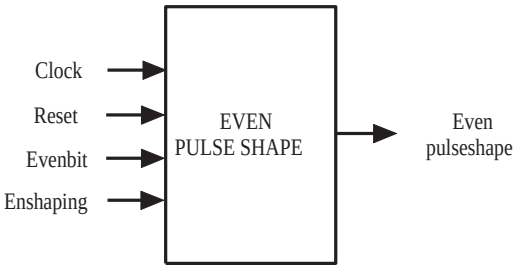
Input Output Description

The I-phase signal and Q-phase signals are pulse shaped by continuous values. In this design the sampling values are fixed integers as mentioned in earlier section. The I/O diagram and description of this module are as follows and the modelsim result is presented

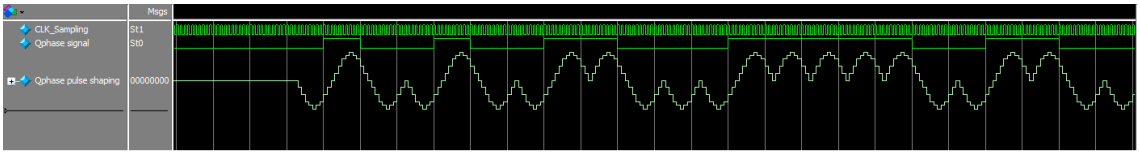
Table 3.5: I/O Description even pulse shape

SL No	PIN Name	Direction	Size	Description
1	Clock(clk50)	Input	1	Synchronous Clock 10 MHz
2	Reset	Input	1	Asynchronous Reset
3	Enshaping	Input	1	Valid Signal for pulse shape
4	Evenbit	Input	1	Evenbit PIN output from serial to parallel module is assigned to this pin
5	Even pulseshape	Output	8	8 bit sample value assigned to this output pin

in 3.21b. This result interprets clock signal of frequency 10 MHz named as 'clk_sampling', Q-phase signal termed as 'Qphase signal'. This signal produces Q-phase pulse shaping signal termed as 'Qphase pulse shaping' after multiplication of sampling values with Q-phase signal. This result shown for simulation time of 270000 ns from top to bottom respectively. Similarly for I-phase signal, pulse shaping description is mentioned in 3.5 with the modelsim results as presented in Figure 3.22b. Figure 3.22b interprets clock signal of frequency 10 MHz named as 'clk_sampling', I-phase signal named as 'Inphase signal' and I-phase pulse shaping signal named as 'Inphase pulse shaping' for simulation time of 270000 ns.

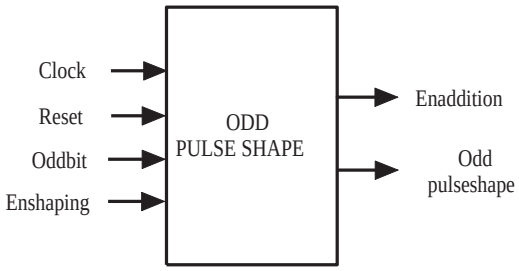


(a) I/O Diagram of Even pulse shaping

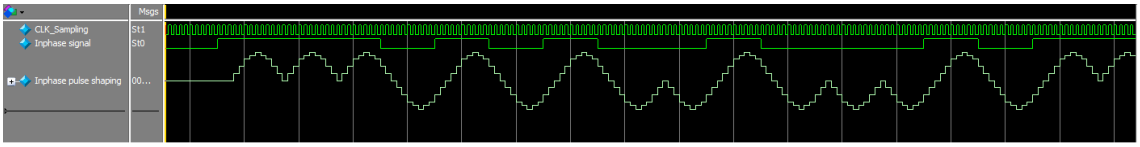


(b) Q-phase pulse shaping(Modelsim Simulation)

FIGURE 3.21: Q-phase pulse shaping



(a) I/O Diagram of Odd pulse shaping



(b) I-phase pulse shaping(Modelsim Simulation)

FIGURE 3.22: I-phase pulse shaping

Table 3.6: I/O Description Odd pulse shape

SL No	PIN Name	Direction	Size	Description
1	Clock(clk50)	Input	1	Synchronous Clock
2	Reset	Input	1	Asynchronous Reset
3	Enshaping	Input	1	Valid Signal for pulse shape
4	Oddbit	Input	1	Oddbit PIN output from serial to parallel module is assigned to this pin
5	Odd pulseshape	Output	8	8 bit sample value assigned to this output pin
6	Enaddition	Output	1	Valid Signal for IQaddition assigned to this output pin

3.4 Baseband Receiver Design for FPGA

This section concentrates on baseband design for synchronous detection of ZigBee transmitter. Input to receiver is the pulse shape signal from the transmitter. The pulse shaping function performed at the transmitter reduces Inter Symbol Interference (ISI). So it has been assumed that the pulse shaping signal is the baseband signal after demodulation at the receiver. The baseband receiver design covers Sample extraction of even bit and odd bit streams, parallel to serial conversion, chip to symbol conversion. The baseband receiver is designed in verilog HDL as per the block diagram presented at Figure 3.23.

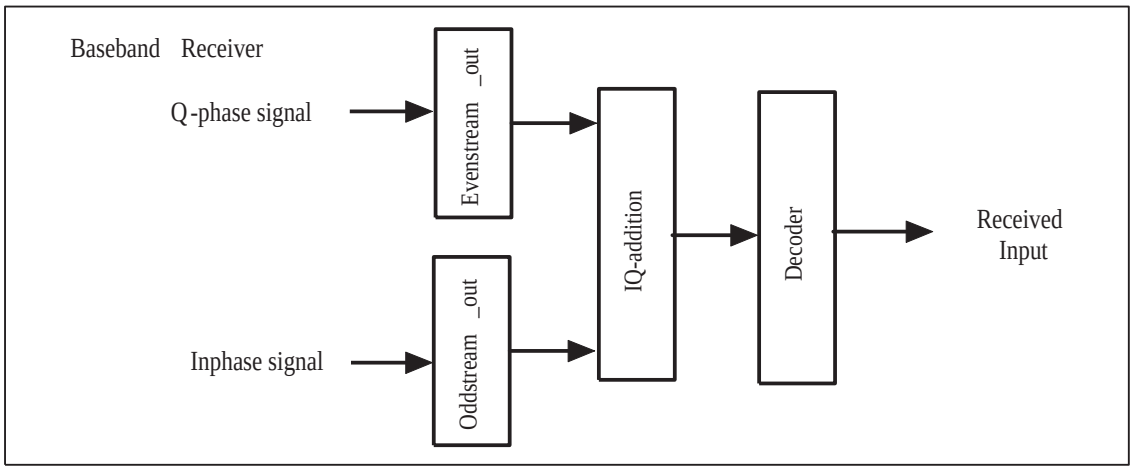


FIGURE 3.23: ZigBee Baseband Receiver

3.4.1 Pulse shape detection

Here, synchronized communication system is assumed. from the received signal the I and Q channels are separated and the evenbit stream and oddbit stream are identified. The pulse output of the transmitter is provided to the input of the baseband receiver for further processing.

3.4.2 Parallel data(even and odd stream)

In verilog HDL design the DCM clock signal clk50 of frequency 10 MHz is used to detect the samples in odd pulse shape and in even pulse shape. So according to the samples in the pulse shape waves the even bit and odd bit streams are detected at receiver. The half bit delay in even bit stream is provided with clock signal clk50, which is same as transmitter clock signal clk50 created by DCM.

Input Output Description

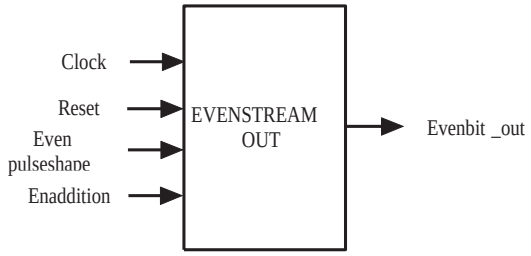
Input output description of I-phase signal and Q-phase signals at receiver are presented in Table 3.7 and 3.8. The I/O diagram and signals are presented at Figure 3.24a to Figure 3.25b. The simulation result shown in Figure 3.24b represents clock signal of frequency 10 MHz named as 'clk50' and the signals 'sampling value' and 'register', which consists of

Table 3.7: I/O Description of Evenstream_out

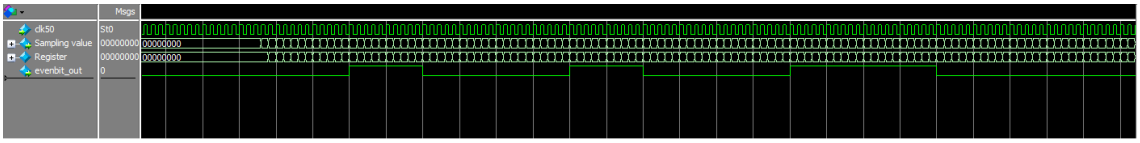
SL No	PIN Name	Direction	Size	Description
1	Clock(CLK50)	Input	1	Synchronous Clock of 10 MHz
2	Reset	Input	1	Asynchronous Reset
3	Even pulseshape	Input	8	8 bit even pulse shape from evenpulseshape module assigned to this pin
4	Enaddition	Input	1	Valid Signal for pulse shape assigned to this pin
5	Evenbit_out	Output	1	Even bit detected from Even pulse shape assigned to this output pin

8 bit sampling values used for pulse shaping and the Q-phase signal at receiver named as 'evenbit_out' for 270000 ns simulation time.

The signals shown in Figure 3.25b represents clock signal of frequency 10 MHz named as 'clk50' and the signals 'Sampling value' and 'QphaseRegister' which shows 8 bit sampling values used for pulse shaping along with the I-phase signal at receiver named as 'oddbit_out' for 270000 ns simulation time.



(a) I/O Diagram of Evenstream_out

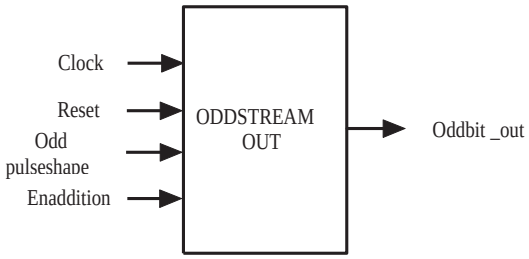


(b) Even data stream at Receiver(Modelsim Simulation)

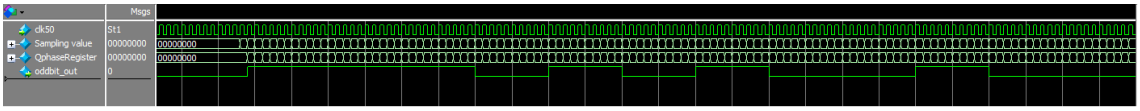
FIGURE 3.24: Q-phase signal at Receiver

3.4.3 Parallel to serial conversion

In this module the two channel 'I' and 'Q' parallel data of 1 Mbps each combined together to form a 2 Mbps serial signal. In HDL design the data bits of I-phase and Q-phase signal



(a) I/O Diagram of Oddstream_out



(b) Odd data stream at Receiver(Modelsim Simulation)

FIGURE 3.25: I-phase signal at Receiver

Table 3.8: I/O Description of Oddstream_out

SL No	PIN Name	Direction	Size	Description
1	Clock(CLK50)	Input	1	Synchronous Clock of 10 MHz
2	Reset	Input	1	Asynchronous Reset
3	Odd pulseshape	Input	8	8 bit odd pulse shape from oddpulseshape module assigned to this pin
4	Enaddition	Input	1	Valid Signal for pulse shape assigned to this pin
5	Oddbit_out	Output	1	Even bit detected from Even pulse shape assigned to this output pin

at receiver are assigned to a 4 bit register alternately. The Figure 3.26 represents the formation of serial data from I-phase and Q-phase signal. The clock signal clk32 is used for parallel to serial conversion, which is used for serial to parallel conversion at transmitter. As per the active edge of clk32 and flag value we are assigning the I-phase and Q-phase data bit to form the 2 Mbps serial data.

Input Output Description

The input and output description of this module with modelsim simulation of serial data is presented in Table 3.9 and Figure 3.27b respectively. The Figure 3.27b presents the clock signal 'clk32' of frequency 1 MHz, I-phase and Q-phase signal respectively termed as 'oddbit_out' and 'evenbit_out' and the received DSSS serial signal at receiver named as

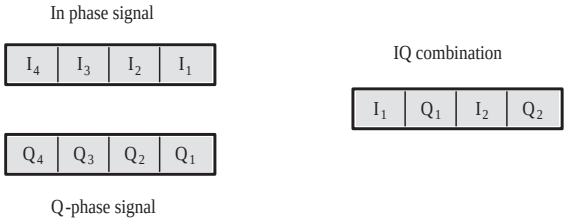
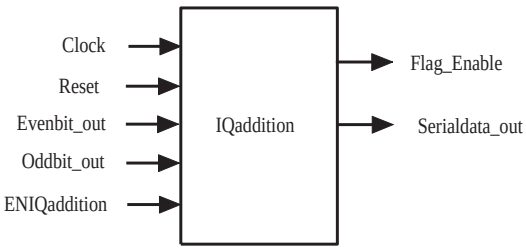
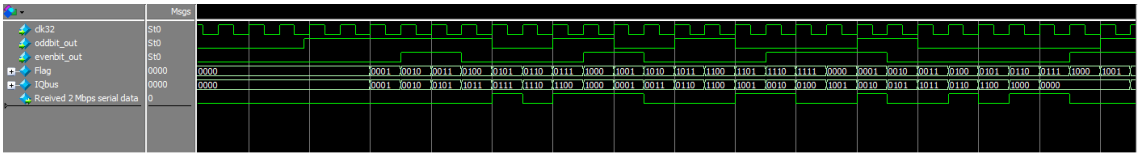


FIGURE 3.26: Parallel to serial conversion at Receiver

'Received 2 Mbps serial data' for simulation time of 270000 ns.



(a) I/O Diagram of IQaddition



(b) IQ Combination at Receiver(Modelsim Simulation)

FIGURE 3.27: I-phase and Q-phase Combination at Receiver

3.4.4 Chip to symbol mapping at receiver

In this module the received 2 Mbps serial data is stored in a 32 bit register with the help of clock signal clk32 generated by DCM, which is used as symbol to chip mapping in transmitter. Here the lookup table used in transmitter for symbol to chip mapping is used in reverse order ie chip to symbol mapping for decoding the received symbol. The received chip sequence is compared with the 16 different chip sequence transmitted by the transmitter. Figure 3.28 demonstrates this process matching. Here, the XNOR operation is carried out on received chip sequence with each of 16 different chip sequences used at transmitter. In XNOR operation, the counter with maximum value provides the symbol

Table 3.9: I/O Description of IQaddition

SL No	PIN Name	Direction	Size	Description
1	Clock(clk32)	Input	1	Synchronous Clock of 1 MHz
2	Reset	Input	1	Asynchronous Reset
3	Evenbit_out	Input	1	one bit data from Evenstream out module assigned to this pin
4	Oddbit_out	Input	1	one bit data from Oddstream out module assigned to this pin
5	ENIQaddition	Input	1	Valid input signal for IQaddition assigned to this output pin
6	Flag_Enable	Output	1	Valid input signal for Chipmapping assigned to this output pin
7	Serialdata_out	Output	1	Combined 2 Mbps serial data after IQ addition, assigned to this output pin

transmitted by the help of lookup table of chip to symbol mapping. This 4 bit symbol is stored in a 4 bit register named as 'dataout', then MSB of 'dataout' is sent to the output as received data bit. The Figure 3.30 shows modelsim simulation result of recovered data bit. This figure displays clock signal of frequency 250 KHz named as 'clk', the received symbol at receiver after chip to symbol mapping is described by a signal of 4 bit register named as 'Symbol_received' and the received signal at receiver is termed as 'Input databit received' which is shown in simulation result over 270000 ns simulation time.

Input Output Description

The 2 Mbps serial data after addition in IQaddition module, is stored in 32 bit flag and the decoding performs in this module. The I/O description of chip to symbol decoding module is presented in Table 3.10. The modelsim simulation result in Figure 3.29b displays chip mapping at receiver. The figure has 16 different chip mapping sequences of 32 bit each, which indicates the correlation of chip sequences at receiver. Out of all chip sequence, the chip sequence has highest matching with received chip sequence is considered as transmitted chip sequence.

The signals in Figure 3.29b represents the clock signal 'clk32' of 1 MHz and 32 bit

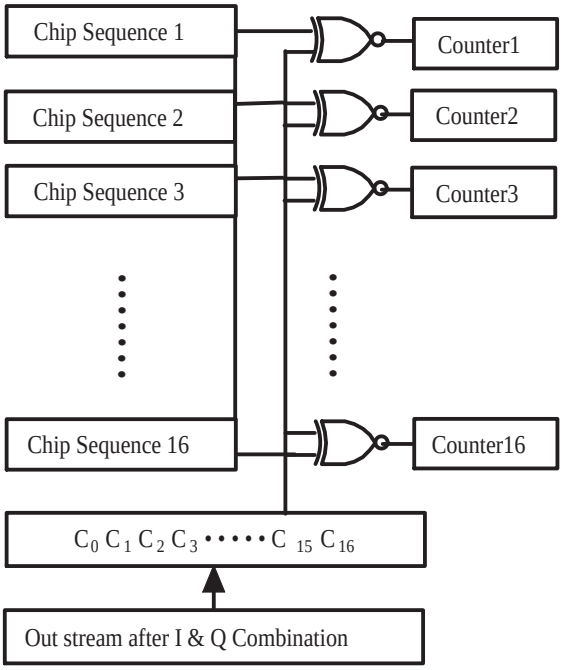
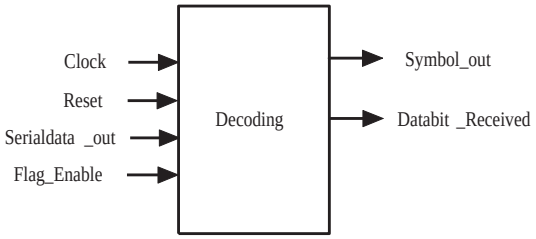


FIGURE 3.28: Decoding at Receiver

register named as 'flag_2Mbps' are shown for 270000 ns simulation time. The signals termed as 'chipmapping1', 'chipmaping2', 'chipmaping3', 'chipmaping4', 'chipmaping5', 'chipmaping6', 'chipmaping7', 'chipmaping8', 'chipmaping9', 'chipmaping10', 'chipmaping11', 'chipmaping12', 'chipmaping13', 'chipmaping14', 'chipmaping15', 'chipmapping16' represents chip mapping output of 'flag_2Mbps' signal with all possible chip sequences of corresponding transmitted symbol and received serial signal of 2 Mbps data rate named as 'Received 2 Mbps serial data' are shown for 270000 ns simulation time.

3.5 FPGA Implementation

After the system level simulation in Simulink, then the module was programmed using hardware description language verilog HDL for simulation. The baseband transceiver module simulated, synthesized and finally implemented on Virtex 5 FPGA. In the process of implementation on FPGA, clock signal generation is very vital [39]. In order to get the required clock signal the digital clock manager available in FPGA was used.



(a) I/O Diagram of Decoding module at Receiver

(b) Chip mapping at Receiver(Modelsim Simulation)

FIGURE 3.29: Chip mapping at Receiver

Table 3.10: I/O Description of Decoding

SL No	PIN Name	Direction	Size	Description
1	Clock(clk)	Input	1	Synchronous Clock of 250 KHz
2	Reset	Input	1	Asynchronous Reset
3	Flag_Enable	Input	1	Valid input signal for decoding assigned to this pin
4	Serialdata_out	Input	1	Combined 2 Mbps serial data from IQaddition module, assigned to this pin
5	Symbol_out	Output	4	4 bit Symbol extracted from decoding module assigned to this output pin
6	Databit_Received	Output	1	MSB of the Symbol is assigned to this output pin which is data bit transmitted

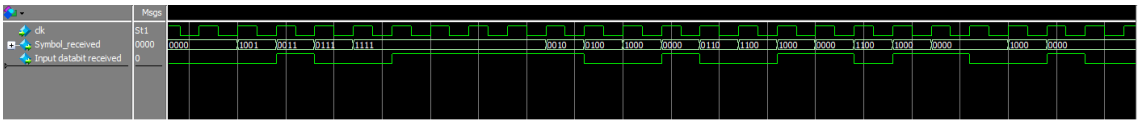


FIGURE 3.30: Received data bit

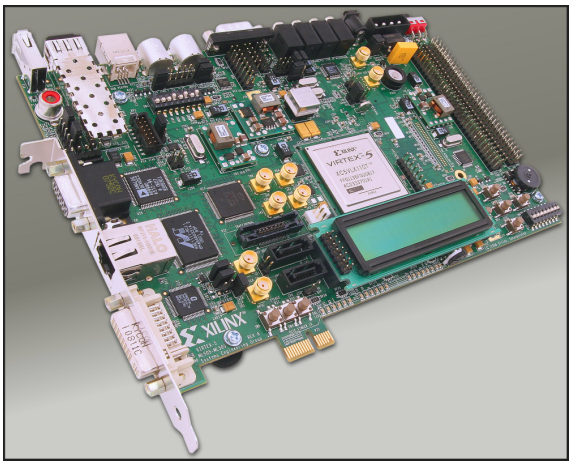


FIGURE 3.31: XILINX VIRTEX 5 FPGA Board with XC5VLX110T

Following verilog simulation of the transceiver, this section presents VIRTEX 5 FPGA board specification, clock circuit generation, synthesis report of implemented design and representation of board internal signals for receiver.

3.5.1 VIRTEX 5 FPGA

The general purpose development board from Xilinx which embeds Virtex 5 FPGA is ML505. This is useful for prototyping on the new architectural features of Virtex-5 FPGA. ML505 contains Virtex-5 XC5VLX110T device [40]. This device contains block RAM, DSP blocks, source synchronous interface block, enhanced clock manager etc. Among all devices of of VIRTEX 5 FPGA family the XC5VLX110T FPGA has higher logic capacity than others. The Table 3.11 shows available resources for LX110T. 100 MHz clock frequency chosen from AH15 pin of FPGA board for generation of clock circuitry [41]. Clock pin description of VIRTEX 5 board is presented in Table 3.12 [41].

Table 3.11: Hardware Resources of VIRTEX 5 LX110T

Slices	**Flipflops**	**LUTs**	**Multipliers**	**Block RAM(Kb)**	CMTs
17280	69120	69120	64	4608	6

Table 3.12: Clock frequency for VIRTEX 5 LX110T

Clock Name	**FPGA PIN**	**Frequency in MHz**
USER_CLK	AH15	100
CLK_33MHz_FPGA	AH17	100
CLK_27_FPGA	AH18	27
CLK_FPGA_P	L19	200
CLK_FPGA_N	K19	200

3.5.2 Digital Clock Manager(DCM)

A properly synthesized clock circuit is essential to achieve implementation task so that the clock signals should be able to reach all the points of the design at the same time. In order to achieve this, a perfectly synchronized clock circuitry was designed by the help of Digital Clock Manager(DCM).

The global clock MUX buffer and clock manager tiles(CMT) provides the solution for designing desired clock network. There are 6 CMTs available on the board, each contains two DCMs and one phase locked loop(PLL) [42].The DCM can generate 90°, 180° and 270° phase-shifted version of external clock. Three different clock frequency signals are generated by using VIRTEX 5 board clock frequency of 100 MHz. The generation of internal clocks of 10 MHz, 1 MHz, 250 KHz is done by using Figure 3.32, where the clock divider factors 10 and 4 are used. This digital clock manager develops clock signal as presented in Figure3.33.

3.5.3 Implementation on VIRTEX 5 FPGA

Xilinx Synthesis Tool (XST) performs the synthesis and optimization in FPGA. During this process following steps are carried out for design, synthesis and optimization:

- Mapping and optimization on an entity by entity or module by module basis
- Global optimization on the complete design

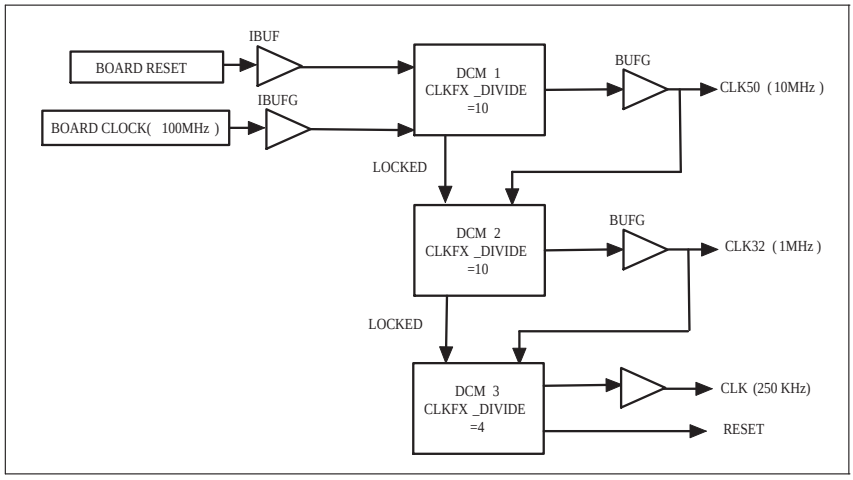


FIGURE 3.32: Digital Clock Manager

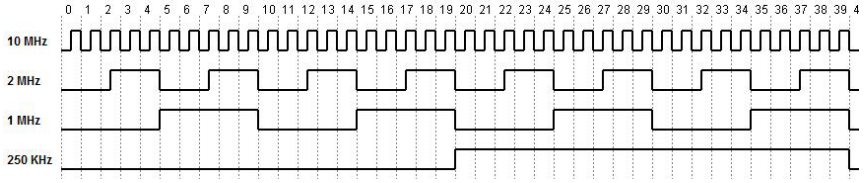


FIGURE 3.33: Digital Clock Manager

The FPGA Device Macro Generator module provides the XST HDL Flow with a catalog of functions. These functions are identified by the inference engine from the Hardware Description Language (HDL) description. Their characteristics are handed to the Macro Generator for optimal implementation. The set of inferred functions ranges in complexity from simple arithmetic operators (such as adders, accumulators, counters and multiplexers), to more complex building blocks (such as multipliers, shift registers and memories). Inferred functions are optimized to deliver the highest levels of performance and efficiency for the selected VIRTEX 5 architecture, and then integrated into the rest of the design. For arithmetic functions, XST provides the following elements:

- Adders, Subtractors and Adder/Subtractors
- Cascadable Binary Counters

- Accumulators
- Incrementers, Decrementers and Incrementer/Decrementers
- Signed and Unsigned Multipliers

Table 3.13 shows the options to fine-tune FPGA synthesis to meet design constraints.

Table 3.14 shows The Device Utilization Summary. Which is the output of HDL synthesis step to estimate the number of slices and gives the number of flip-flops, IOBs.

Table 3.15 shows the advanced synthesis report, which includes XST additional macro processing by improving the macros recognized at the HDL synthesis step, or by creating the new, more complex ones, such as dynamic shift registers. The implemented design in VIRTEX 5 LX110T FPGA board has maximum clock frequency of 11.792 MHz and maximum output required time is 3.264 ns. The total logic power consumed by the design is 0.45 mW.

3.5.4 Synthesis Report

The internal signals along with received baseband data was analyzed through ChipScope Pro analysis. The received I-phase, Q-phase and baseband data bit received signal are analyzed as depicted in Figure 3.34. The top level RTL schematic of this transceiver obtained from the ISE design environment is presented in Figure 3.35.

Table 3.13: Synthesis options summary

Synthesis options summary	
Input File Name	"datain_tb.prj"
Input format	mixed
Ignore Synthesis Constraint File	No
Output File name	"datain_tb"
Automatic FSM Extraction	YES
FSM Encoding Algorithm	No
FSM Style	LUT
RAM Extraction	Yes
RAM Style	Auto
Rom Extraction	Yes
Mux style	Auto
Decoder Extraction	YES
Priority Encoder Extraction	Yes
Shift Register Extraction	Yes
Logical Shifter Extraction	Yes
Mux Extraction	Yes
Resource Sharing	YES
Use DSP Block	Auto

Table 3.14: Device Utilization Summary

Slice Logic Distribution		
Number of Slice Registers	973 out of 69120	1%
Number of Slice LUTs	1179 out of 69120	1%
Number used as logic	1178 out of 69120	1%
Number used as Memory	1 out of 17920	0%

I/O Utilization		
Number of bonded IOBs	8 out of 640	1%
Number of BUFG/BUFGCTRLs	10 out of 32	31%
Number of DCM_ADVs	3 out of 12	33%

Table 3.15: Advance HDL Synthesis Report

Advance HDL Synthesis Report	
ROMs	1
128x1-bit ROM	1
Adders/Substracters	32
6-bit adder	32
Counters	6
2-bit up counter	1
4-bit up counter	2
5-bit up counter	2
7-bit up counter	1
Registers	711
Flip-Flops	711
Latches	545
Comparators	48
Multiplexers	1

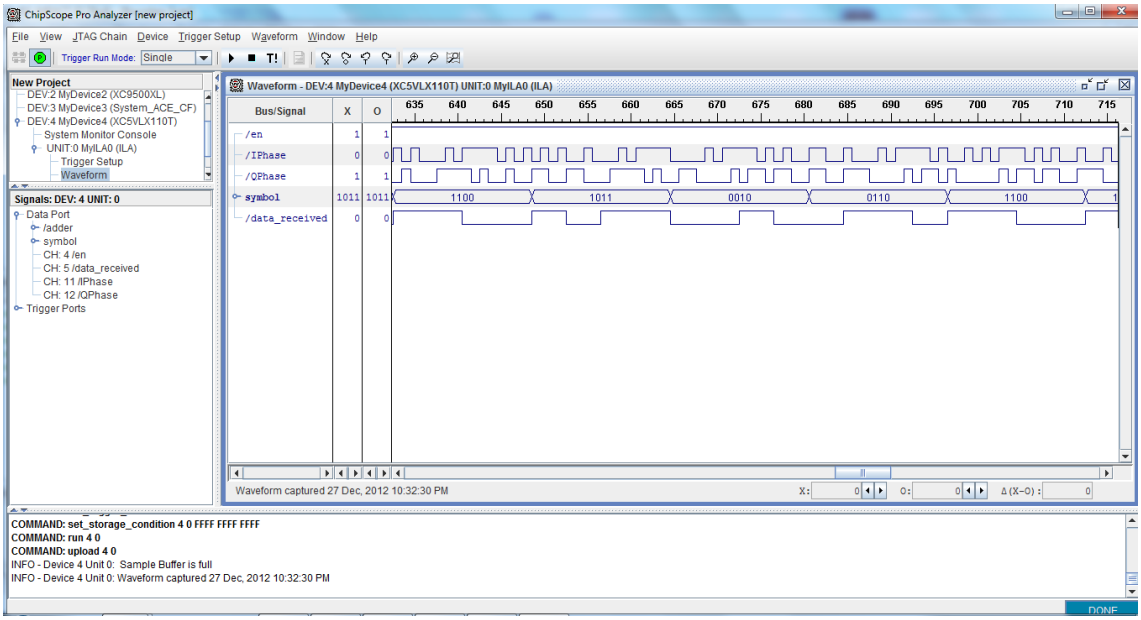


FIGURE 3.34: ChipScope Pro Internal signals

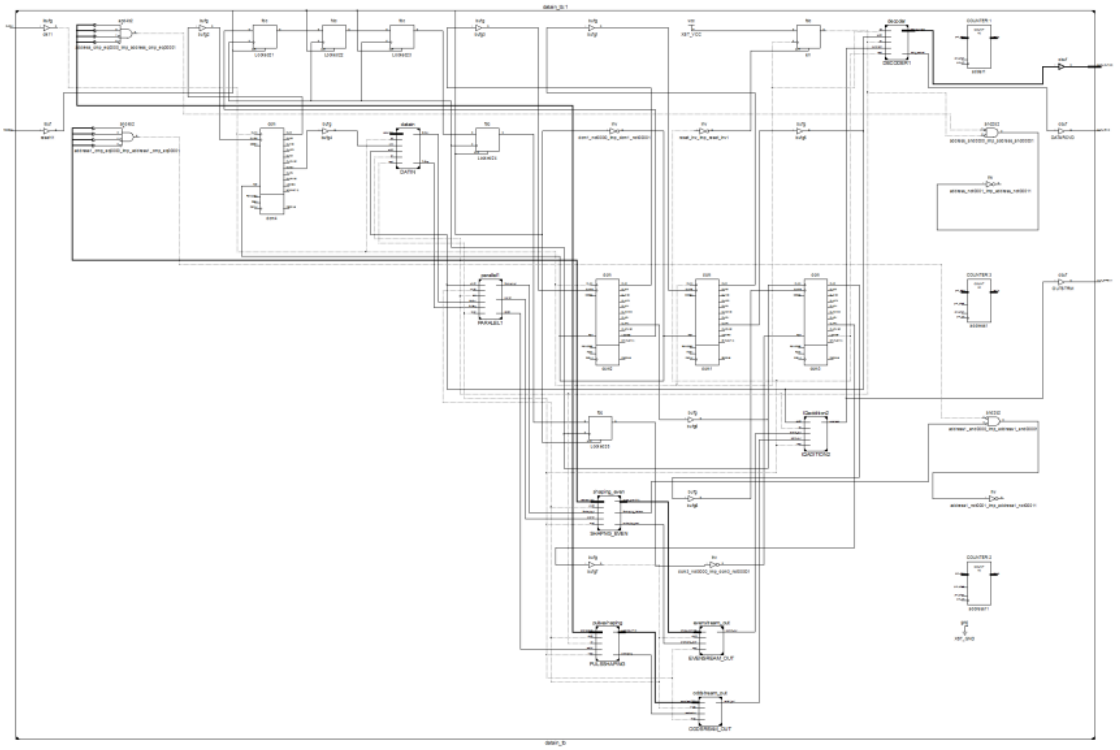


FIGURE 3.35: Top level RTL Schematic of ZigBee Baseband Transceiver

3.6 Summary and Discussion

ZigBee baseband transceiver for IEEE 802.15.4 was implemented through various stages which include.

- Initially the transceiver system simulated through MATLAB/Simulink, where Minimum shift keying(MSK) modulation technique is used. The internal signal of different stages of simulink model are analyzed.
- The baseband module is described in hardware description language verilog HDL and simulated in mentor graphics modelsim simulator and finally realized in Virtex 5 FPGA using ISE design environment. The system provided desirable performance. The simulation result presented above are labeled as X-axis in time(ns) and Y-axis presents the respective signals.
- Following this, in FPGA implementation, the clock signals of 250 KHz, 1 MHz, and 10 MHz were derived by taking 100 MHz clock signal available on Virtex 5 FPGA board. Further the design synthesis report along with board internal signals were also analyzed for verification.
- In XILINX power analysis, the total power consumption for the ZigBee baseband transceiver is reported to be 0.45 mW. The detail power analysis of logic power and signal power at each stage of the design reported by the ISE synthesizer is as follows.

Table 3.16: Hierarchical power analysis

Name	**Power(w)**	**Logic Power(w)**	**Signal Power(w)**
Hierarchical Total Power	0.21672	0.21350	0.000322
Datain_tb	0.21401/0.21672	0.21317/0.21350	0.00084/0.00322
Decoder Module	0.00163	0.00007	0.00156
Evenstream_out	0.00009	0.00004	0.00006
Parallel1	0.00009	0.00002	0.00007
IQADDITION2	0.00011	0.00002	0.00009
SHAPING$_EVEN$	0.00012	0.00004	0.00008
ODDSTREAM_OUT	0.00012	0.00003	0.00009
PULSHAPING	0.00015	0.00005	0.00010
DATAIN	0.00037/0.00039	0.00004/0.00006	0.00033

4

ZigBee Transceiver Design with RNS Based PN sequence

In this chapter the design of a new form of ZigBee transceiver is presented. This transceiver uses residual number system based PN sequence instead of the chip sequence used in 2.4 GHz ZigBee for IEEE 802.15.4. This chapter introduces Residue Number System(RNS) in brief as presented in following section.

4.1 Residue Number System

Residue Number System (RNS) has become very popular in recent time due to their superior performance in terms of large dynamic range, good cross correlation and auto correlation properties. The chapter discusses advantages of RNS which in turn motivated us to take up the work.

In Residue number system, a number X is represented by a set of residues like $x_1, x_2, ..x_n$, modulo given by co-prime moduli. The moduli set is known as the system base and residues are known as residue digits. The dynamic range of the system ie the number of possible number representation is defined by the product of all RNS moduli. In this numbers system, addition, multiplication, substraction can be used without carry propagation between residue digits, which enables arithmetic circuits to perform faster than the circuits for binary representation. This property permits to build arithmetic units of large numbers as

a set of fast and small circuits [43].

The important merit of RNS over conventional number number system is the absence of carry propagation in addition and multiplication. In other number systems after an operation if carry is generated than it is forwarded to the next bit of the operand. In RNS, low precision is required for ranging to individual prime and co-prime number of moduli-set, subsequently it enables lookup table implementation for different operations. Due to lookup table the operation speed of RNS is faster with lower computational complexity and hence low power consumption. These two features are expected to be advantageous for VLSI implementation.

4.1.1 Chinese Remainder Theorem

Chinese Remainder Theorem(CRT) is a mathematical formulation used to find independent unique numbers in a given dynamic range. In RNS CRT has an important role to play, so as to find RNS representation of a number. CRT implies that if moduli of RNS is chosen accurately then each number can be uniquely represented in the given dynamic range. In other words CRT states that if all the divisors are co-prime to each other then the residue representation of each number is different to each other or unique in the dynamic range $'R'$. Here $'R'$ is the multiplication of all the divisors or modulis of the moduli-set. Since the set of divisors or modulis are not fixed, if the set of divisors increases then the bit representation in RNS will be increased proportionately.

Assume a_1 and a_2 are two integers which are relatively prime to each other and b_1 and b_2 are any two integers, then there is an integer N can be determined by 4.1 and 4.2.

$$N \equiv b_1 (mod\ a_1) \tag{4.1}$$

$$N \equiv b_2 (mod\ a_2) \tag{4.2}$$

N is an uniquely determined modulo $(a_1.a_2)$. Equivalently if $gcd\ (a_1, a_2) = 1$, then the pair of residue classes modulo a_1 and a_2 corresponds to a simple residue class modulo

(a_1, a_2) which gives a simultaneous congruences $b \equiv b_i(mod\ a_i)$, for $i = 1, 2, 3....b$ for which a_i are relatively prime. Then, the solution to set of congruences is given by (4.3).

$$z = x_1 * y_1 \frac{A}{a_1},\ x_2 * y_2 \frac{A}{a_2},\ ....\ x_p * y_b \frac{A}{a_n} \tag{4.3}$$

where $A = a_1, a_2....a_n$ and y_i is determined from $y_1 \frac{A}{a_1} = 1(\mod a_1)$

4.1.2 Arithmetic in RNS

Residue number system completely depend on the congruence relation of the number. Two numbers are said to be congruent modulo 'm' if the number 'm' divides exactly the difference of a and b ie $(a - b)$, then mathematically congruent modulo of a and b is represented as $a \equiv b(mod\ m)$. for example $15 \equiv 12(mod\ 3), 10 \equiv 6(mod\ 2), 11 \equiv 2(mod\ 3)$ etc.

The RNS gives separate unique representation for all numbers in the range between 0 and $M - 1$. If the given integer number is greater than $M - 1$, then RNS representation of the integer is the integer itself. Therefore, more than one integer may have the same residue representation. Before this, it should be confirmed that the moduli have to be relatively prime to be able to exploit the dynamic range. The example of residue representation shown in Table 4.1 provides the principle as per Chinese Remainder Theorem (CRT)[44].

Choice of Moduli

By the mathematical perspective the best moduli are the prime numbers. If 'm' is prime, then there must be one generator, $p \leq m - 1$. then the set of all non-zero residue with respect to 'm' is given by relation (4.4). There are two approach of moduli selection, one is consecutive method and the other is arbitrary method [16, 43]. The proposed PN sequence is generated on the basis of consecutive method of moduli-set selection [15], here the moduli-set [255 254 253 251] is selected for generation of RNS based PN sequence for transceiver design.

Table 4.1: Residue Representation in RNS

N	Relative Prime Moduli			Relative Non-Prime Moduli		
	$m_1 = 2$	$m_2 = 5$	$m_3 = 7$	$m_1 = 2$	$m_2 = 4$	$m_3 = 6$
0	0	0	0	0	0	0
1	1	1	1	1	1	1
2	0	2	2	0	2	2
3	1	3	3	1	3	3
4	0	4	4	0	0	4
5	1	0	5	1	1	5
6	0	1	6	0	2	0
7	1	2	0	1	3	1
8	0	3	1	0	0	2
9	1	4	2	1	1	3
10	0	0	3	0	2	4
11	1	1	4	1	3	5
12	0	2	5	0	0	0
13	1	3	6	1	1	1
14	0	4	0	0	2	2
15	1	0	1	1	3	3
16	0	1	2	0	0	4
17	1	2	3	1	1	5
18	0	3	4	0	2	0
19	1	4	5	1	3	1
20	0	0	6	0	0	2
21	1	1	0	1	1	3
22	0	2	1	0	2	4
23	1	3	2	1	3	5
24	0	4	3	0	0	0
25	1	0	4	1	1	1
26	0	1	5	0	2	2
27	1	2	6	1	3	3
28	0	3	0	0	0	4

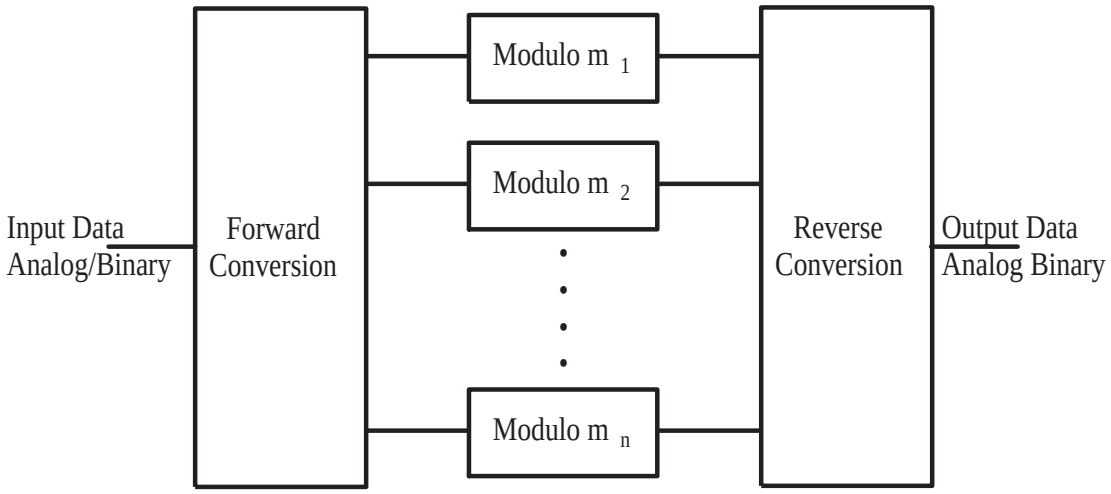


FIGURE 4.1: Basic Structure of RNS Processor

$$Residue = |p^i|_m : i = 0, 1, 2, ..., m-2 \tag{4.4}$$

if $m = 7$ and $p = 5$ then residues are calculated as $|5^0|_7 = 1,\ |5^1|_7 = 5,\ |5^2|_7 = 4,\ |5^3|_7 = 6$

4.1.3 Structure of RNS Conversion

The basic structure of a typical RNS processor is shown in Figure 4.1. The RNS data processed in parallel according to the concept of residue number system independently without carry propagation. In RNS processor encoding of input data to RNS is called forward conversion and decoding of RNS to conventional number representation is known as reverse conversion.

For full RNS based system the analog input number first converted to binary form then the residue of the number calculated during forward conversion and residue number to binary representation during reverse conversion. During processing, conversion to binary is an intermediate stage which is required in both forward and reverse conversion. This makes the conversion inefficient due to increased latency and complexity.

Arbitrary Moduli-set forward conversion

The special moduli-set such as $2^n - 1, 2^n, 2^n + 1$ is help full for making forward conversion process fast and simple. The special moduli-set forward converters are more efficient converters. Other than this large dynamic range requirement in some applications can not be provide with efficient special moduli-set, which in turn demands an arbitrary moduli-set forward conversion.

Arbitrary moduli-set forward conversion can be implemented by using lookup tables or combinational logic. Implantation of converter with combinational logic makes the processing unit complex, so the lookup table implementation is preferred over combinational logic. Implementation of large dynamic range increases the ROM size and simultaneously the conversion process becomes inefficient. Therefore a tradeoff between the two implementations can be utilized using a combination of lookup table and combinational logic[45, 16].

For ZigBee application standard 16 different PN codes of length 32 bit are required. The process of generation of the code is discussed in succeeding section. Table4.2.

4.2 RNS Based PN Sequence for ZigBee Spreading and Despreading

In this section the residue number system(RNS)[16] based PN sequence generation is analyzed. A set of new PN sequence based on RNS is proposed for ZigBee baseband transceiver, which is used in ZigBee baseband transceiver design for spreading and despreading. The algorithm to generate PN sequence is as follows and the generated PN sequence is presented in Table 4.2.

Algorithm 1 RNS Based PN sequence Generation

1: Take a dynamic Range for primal generation
2: Selection of moduli set
3: For each primal generated above calculate the residue for each of the moduli
4: Convert the set of residues obtained from step 3 to their equivalent 8 bit binary representation
5: Concanate all the binary representation of residues called as PN sequence
6: After obtaining set of PN sequences check for the cross correlation for a specified threshold
7: The sequences satisfying above condition will be selected as RNS Based PN sequence.

4.2.1 RNS Generated PN sequence

Residue Arithmetic based PN sequence generation for multiple scenario are mentioned here. The inputs to the block of RNS generation consists of spread factor β and the cross correlation threshold, T. A moduli set is selected according to the requirement of no of bits in PN sequence. The moduli set is selected either by consecutive method or by exponential method [15]. Here the consecutive method was adopted.

As mention above the Primal is randomly selected from the range R given by $R = \prod_{i=1}^{n} p_i$, where p is the moduli set and is represented as $p = \{p_1, p_2, p_3, \ldots, p_n\}$. Let A be a set of primals chosen from range R and is expressed as $A = x_1, x_2, x_3, \ldots, x_n$. Defining J to be set of residues given by $J_{(i,j)} = |x_j, p_j|$ for $i = 1, 2, \ldots, n$ and $j = 1, 2, \ldots, k$. J can be represented as.

$$J = \begin{pmatrix} mod(x_1, p_1) & mod(x_1, p_2) & . & . & . & mod(x_1, p_n) \\ . & . & . & . & . & . \\ mod(x_n, p_1) & mod(x_n, p_1) & . & . & . & mod(x_n, p_1) \end{pmatrix} \tag{4.5}$$

Each row of J is then represented by 8 bit binary representation. The entire row is termed as desired length of the PN sequence. Hence the generated sequences are tested for their cross correlation as following.

- Correlation between c_i *and* c_j for $i = j$ will be one.
- Correlation between c_i *and* c_j for $i \neq j$ must be less than a threshold value T. The value of T can vary depending on the application, here for 32 bit PN sequence generation threshold $T = 1.5$ is considered to be desirable. This process is repeated till the required number of PN codes are generated.

4.3 Performance of RNS based PN sequence in ZigBee Transceiver

The modern transceivers have to meet the various customer requirements like high capacity, high bandwidth efficiency at variable bit rate. On the other hand wireless environment

Table 4.2: Symbol to Chip Mapping using RNS code for 2.4 GHz ZigBee Transceiver

Data Symbol(Binary)	**Chip values** ($C_0\ C_1\ \ldots\ C_{31}$)
0000	11101011111011101111000111110111
1000	11001101110101001101101111101001
0100	11010110110111011110010011110010
1100	10111111110010101101010111101011
0010	11000000110010111101011011101100
1010	10011100101010111011101011011000
0110	10101010101110011100100011100110
1110	11111011000011110010001001001000
0001	10011001101011001011111111100101
1001	10100001101101111100110111111001
0101	11011001111011110000100000110110
1101	00101000001111110101011010000100
0011	01101110100001011001110011001010
1011	10101111110010011110001100011100
0111	10111001110100111110110100100110
1111	11100111000000110001111001010100

signals are usually impaired by fading and multi path delay spread phenomenon, due to which the mobile communication system do not perform well. In channels with extreme fading causes Inter Symbol Interference (ISI), results in high probability of errors and subsequently system's overall performance becomes very poor.

The next generation short range wireless communication need to be of higher standard in order to provide the customer different short communication like little message transfer and some command transfer. In this section the ZigBee baseband transceiver performance is analyzed in Additive White Gaussian Noise (AWGN) channel and Rayleigh fading channel. Here the performance of the transceiver is tested by replacing the given PN code in the standard IEEE 802.15.4 with the newly generated RNS based PN code. Performance evaluation was carried out through BER simulation using MATLAB software. The BER performance of two types of transceivers using standard code and RNS based code for AWGN channel and Rayleigh fading channel is presented in Figure 4.2 and 4.3 respectively.

BER simulation suggests that RNS based ZigBee performs better than standard code

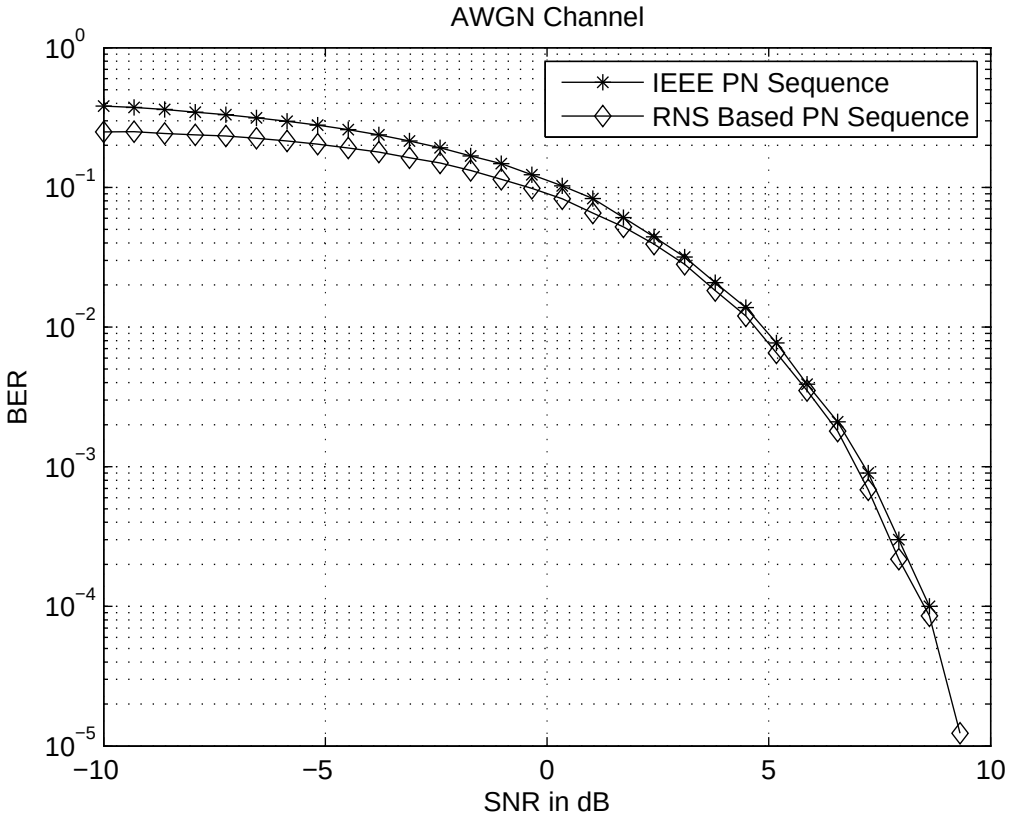


FIGURE 4.2: Performance in AWGN Channel

based ZigBee transceiver. Following this the FPGA based implementation is considered next.

4.4 RNS Based Baseband Transceiver in FPGA

The design principle adopted in 2.4 GHz ZigBee as discussed in chapter 3 is also used here. Here, RNS based PN sequence is used in transceiver design for spreading. Hence sixteen different PN sequences are mapped into sixteen different symbols in a lookup table as presented in Table 4.2. In line with description given in chapter 3, the baseband module is described in HDL. The HDL structure implemented has been presented in Figure 3.17 and comprises of blocks input data stream, bit to symbol mapping, PNsequence,serial to parallel conversion, pulse shaping, parallel to serial conversion etc. Here a minor modification

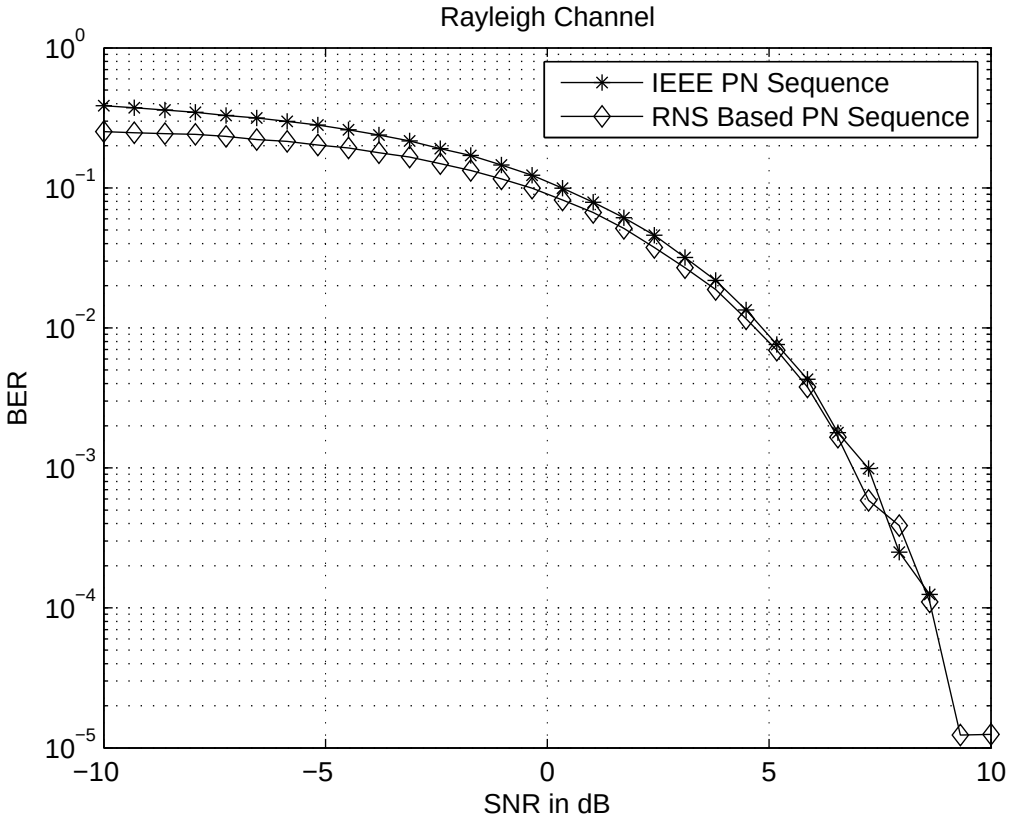
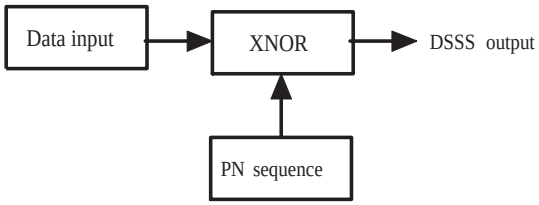


FIGURE 4.3: Performance in Rayleigh fadding Channel

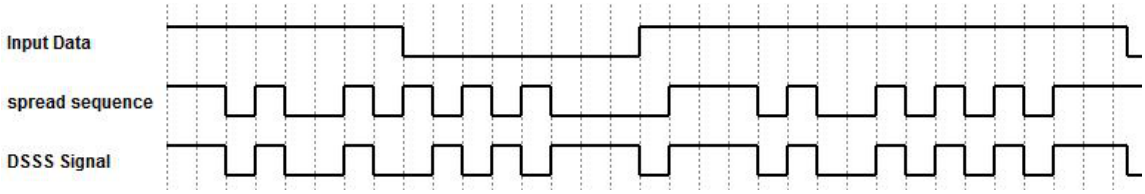
is adopted during symbol to chip conversion, where we perform direct sequence spread spectrum of RNS based PN sequence with respective symbol and rest of all simulation model is same.

Figure 4.4a shows that the DSSS signal obtained by doing digitally XNOR operation of symbol with respective PN sequence. The DSSS signal is of 2 Mbps serial data, and is converted to two 1 Mbps parallel data, In verilog HDL design the PNSEQUENCE module of chapter 3 consists of output pin 'Serial Data' , which is the DSSS output for RNS based PN sequence. This signal is processed as serial to parallel conversion in this section.

RNS based transceiver is designed in a similar way as done in previous chapter. The clock signals CLK, CL32 and CLK50 are derived from the crystal by using digital clock manager. The verilog HDL module of the baseband transceiver is simulated in modelsim



(a) DSSS Operation



(b) pnsequence

FIGURE 4.4: DSSS Operation

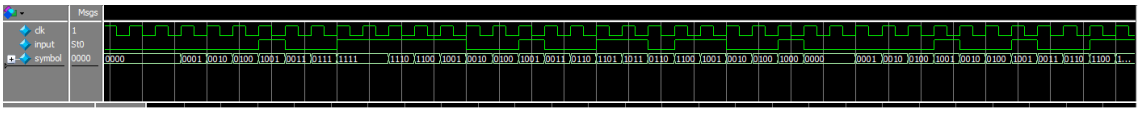
simulator as per the description and input output diagram described in previous chapter.

4.4.1 Simulation Result

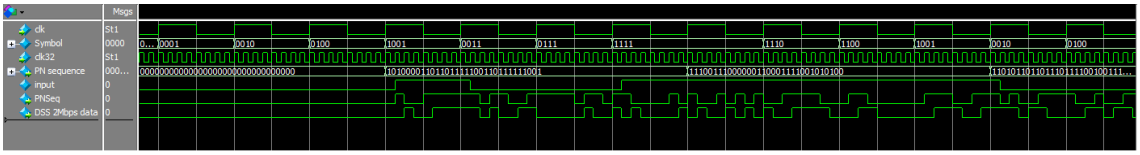
Bit to Chip Conversion

The incoming input data bit is converted to symbol using the datain module and the pnsequence module performs symbol to chip mapping. thereafter DSS signal of 2 Mbps is obtained as output for serial to parallel conversion. These signals are presented in Figure 4.5a and 4.5b.

The Figure 4.5a represents the clock signal of frequency 250 KHz named as 'clk', the incoming data bit 'input' of 250 Kbps data rate and four bit symbol named as 'symbol' for 270000 ns simulation time. The Figure 4.5b displays signals such as clock signal of frequency 250 KHz named as 'clk', data symbol consists four input data bit named as 'symbol', clock signal of frequency 1 MHz named as 'clk32', 32 bit RNS based PN sequence in 32 bit register inside the PNSEQUENCE module named as 'PN sequence', the incoming input data of 250 Kbps named as 'input' , serial PN sequence signal named as 'PNSeq' and 2 Mbps direct sequence spread spectrum signal named as 'DSSS 2 mbps data' for 270000 ns simulation time.



(a) Bit to symbol in modelsim for RNS



(b) Symbol to Chip for RNS

FIGURE 4.5: Bit to Symbol to Chip Conversion for RNS

Serial to Parallel conversion

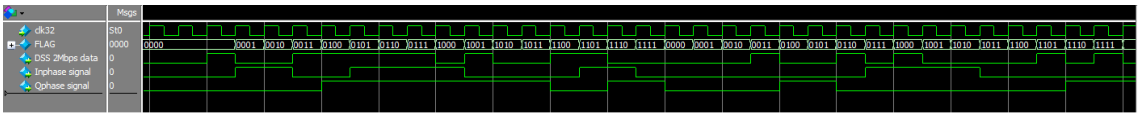
The DSSS output of 2 Mbps signal is separated into two 1 Mbps signal of even bit and odd bits named as I-phase signal and Q-phase signal, which form the input to I-phase pulse shaping and Q-phase pulse shaping networks.

The Figure 4.6a shows the signals such as clock signal 'clk32' of 1 MHz, 4 bit register internal signal containing four bits of DSSS signal named as 'FLAG', the spread spectrum signal of 2 Mbps data rate named as 'DSSS 2 Mbps data', I-phase signal termed as 'Inphase signal' and Q-phase signal termed as 'Qphase signal' for 270000 ns simulation time.

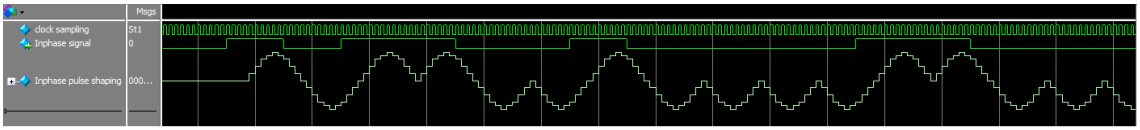
The signals shown in Figure 4.6b represents the clock signal of frequency 10 MHz named as 'clock sampling' used for pulse shaping, I-phase signal named as 'Inphase signal' and I-phase pulse shaping signal termed as 'Inphase pulse shaping' for simulation time of 270000 ns. Similarly the signals in Figure 4.6c describes 10 MHz clock signal named as 'clock sampling' used for pulse shaping, Q-phase signal named as 'Qphase signal' and Q-phase pulse shaping signal termed as 'Qphase pulse shaping' for simulation time of 270000 ns.

Parallel to Serial conversion

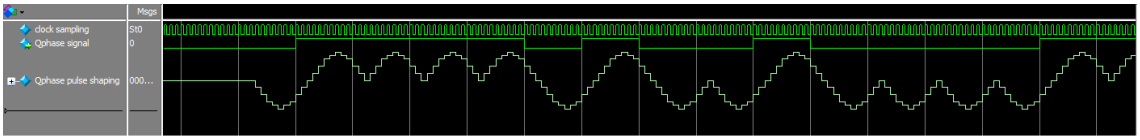
From digital clock manager clock signal 'clk32' is used for addition of I-phase and Q-phase signal at the receiver. Combined I-phase and Q-phase signal forms 2 Mbps serial data, which is the DSSS signal transmitted by transmitter and is presented in Figure 4.7c. This figure displays 1 MHz clock signal named as 'clk32', I-phase signal 'oddbit_out', Q-phase



(a) Serial to Parallel in modelsim for RNS



(b) I-phase pulse shaping for RNS



(c) Q-phase pulse shaping for RNS

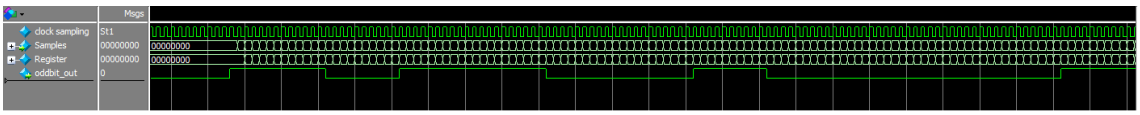
FIGURE 4.6: Pulse shaping of RNS based Transceiver

signal 'evenbit_out', two 4 bit register to store I-phase and Q-phase signal at receiver namely 'FLAG' and 'IQbus'. The out put of this subsystem is received spread spectrum signal of 2 Mbps named as 'Received 2 Mbps DSSS signal'. all these signals described for 270000 ns simulation time.

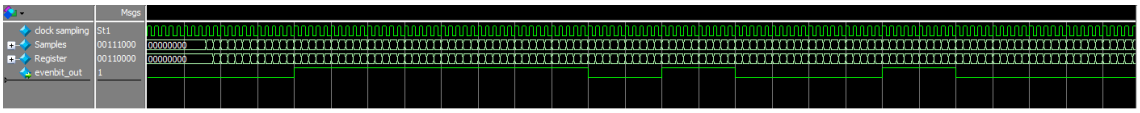
The signals in Figure 4.7a represents 10 MHz clock signal named as 'clock sampling' and I-phase signal received at receiver termed as 'oddbit_out' with the help of two 8 bit registers named as 'samples' and 'Register' used for sample detection at receiver. This result shown for 270000 ns simulation time. Similarly the signals in Figure 4.7b shows the clock signal 'clock sampling' of 10 MHz and Q-phase signal at receiver termed as 'evenbit_out' for 270000 ns simulation time.

Chip to symbol mapping

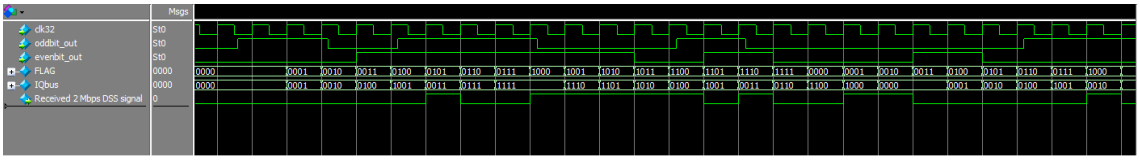
The received chip sequence is first stored in 32 bit register for decoding. The clock signal 'clk32' is used for this purpose. XNOR operation performed between the received sequence and 16 numbers of 32 bit transmitted sequences. From output of this the sequence with highest matching with original received chip sequence is selected and is again mapped to four bit symbol from a lookup table producing desired symbol. The result of chip to symbol



(a) Q-phase signal at Receiver in modelsim for RNS



(b) I-phase signal at Receiver for RNS



(c) DSSS serial signal at Receiver for RNS

FIGURE 4.7: DSSS signal at Receiver for RNS based Transceiver

mapping in modelsim is presented in Figure 4.9a.

Figure 4.9a represents the signals such as clock signal 'clk32' of 1 MHz and 32 bit register named as 'flag_2Mbps' are shown for 270000 ns simulation time. The signals termed as 'chipmapping1', 'chipmaping2', 'chipmaping3', 'chipmaping4', 'chipmaping5', 'chipmaping6', 'chipmaping7', 'chipmaping8', 'chipmaping9', 'chipmaping10', 'chipmaping11', 'chipmaping12', 'chipmaping13', 'chipmaping14', 'chipmaping15', 'chipmapping16' represents chip mapping output of 'flag_2Mbps' signal with all possible chip sequences of corresponding transmitted symbol and received spread spectrum signal of 2 Mbps data rate named as 'Received 2 Mbps DSS signal' are also shown for 270000 ns simulation time. The signals in Figure 4.9b displays clock signal of frequency 250 KHz named as 'clk', the received symbol after chip to symbol mapping is designated by signal of 4 bit register named as 'Symbol_RNS' and the received signal at receiver is termed as 'Input data received' for 270000 ns simulation time.

4.5 Implementation on VIRTEX 5 FPGA

The transceiver for RNS based PN sequence was next implemented on VIRTEX 5 FPGA board. The system used the digital clock manager circuit presented in Figure 3.32 as used

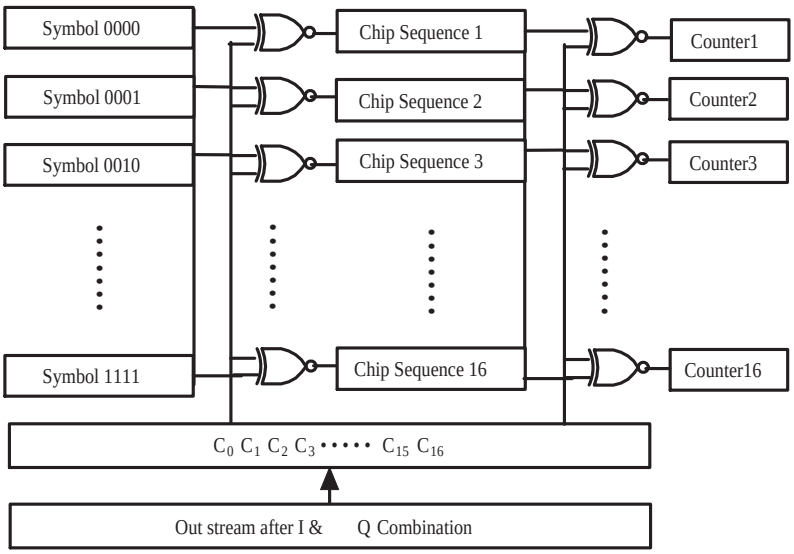
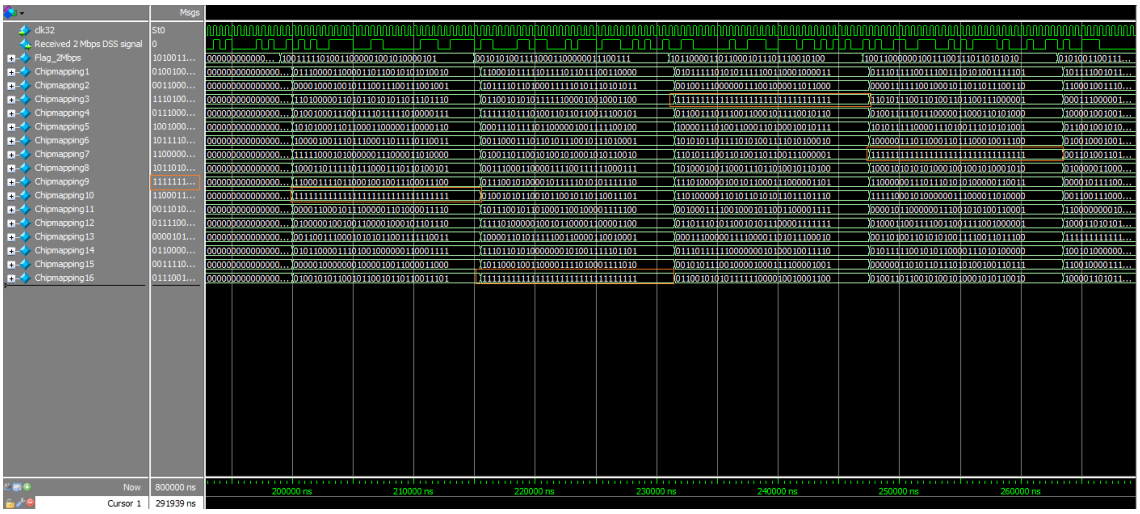
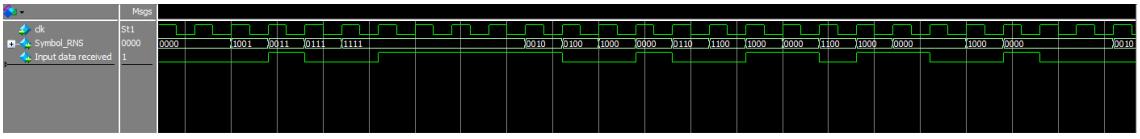


FIGURE 4.8: Decoding of RNS Based Transceiver



(a) Chip Mapping in modelsim for RNS



(b) Data bit received for RNS

FIGURE 4.9: Decoder for RNS based transceiver

in chapter 3. In this design a little extra logic is implemented in comparison to chapter 3 because here the PN sequence is used for Direct sequence spread spectrum baseband modulation for both transmitter and receiver, It is found that most of synthesis report result is similar to results reported in chapter 3 with little variation. Similar to chapter 3 different parameters of synthesis results for this design on FPGA presented here.

The synthesis options to fine-tune FPGA synthesis to meet design constraints of RNS based baseband transceiver is listed in Table 4.3. The device utilization summary analyzed in Table 4.4 which estimates the number of slices, buffers, DCM etc of VIRTEX 5 FPGA board and the Table 4.5 represents advance synthesis report.

The implemented design in VIRTEX 5 LX110T FPGA board has maximum clock frequency of 11.792 MHz and maximum output required time is 3.264 ns. The total logic power consumed by the design is 0.45 mW.

4.5.1 Synthesis Report

The RNS based transceiver design is synthesized in ISE design environment which is reported as follows. It is observed that, in this design there is some differences in slice logic distribution and advance synthesis report as presented below. After synthesis the programming bit file is generated which is downloaded to Virtex 5 LX110T FPGA. The FPGA board internal signals along with received baseband data was analyzed through ChipScope Pro analyzer software of XILINX synthesizer. The internal I-phase, Q-phase, 2 Mbps serial signal at receiver and baseband data bit received signal are observed as depicted in Figure 4.10.

4.6 Summary and Discussion

ZigBee baseband transceiver for RNS based PN sequence was implemented through various stages. The contribution from the chapter can be listed as under.

- The new RNS based PN sequence was used in DSSS transmitter and receiver for the design, this was further simulated in modelsim simulator.

Table 4.3: Synthesis options summary

Synthesis options summary	
Input File Name	"datain_tb_RNS.prj"
Input format	mixed
Ignore Synthesis Constraint File	No
Output File name	"datain$_t b$"
Automatic FSM Extraction	YES
FSM Encoding Algorithm	No
FSM Style	LUT
RAM Extraction	Yes
RAM Style	Auto
Rom Extraction	Yes
Mux style	Auto
Decoder Extraction	YES
Priority Encoder Extraction	Yes
Shift Register Extraction	Yes
Logical Shifter Extraction	Yes
Mux Extraction	Yes
Resource Sharing	YES
Use DSP Block	Auto

Table 4.4: Device Utilization Summary

Slice Logic Distribution		
Number of Slice Registers	988 out of 69120	1%
Number of Slice LUTs	1186 out of 69120	1%
Number used as logic	1185 out of 69120	1%
Number used s Memory	1 out of 17920	0%

I/O Utilization		
Number of bonded IOBs	8 out of 640	1%
Number of BUFG/BUFGCTRLs	10 out of 32	31%
Number of DCM_ADVs	3 out of 12	33%

Table 4.5: Advance HDL Synthesis Report

Advance HDL Synthesis Report	
ROMs	1
128x1-bit ROM	1
Adders/Substracters	32
6-bit adder	32
Counters	6
2-bit up counter	1
4-bit up counter	2
5-bit up counter	2
7-bit up counter	1
Registers	717
Flip-Flops	717
Latches	551
Comparators	58
Multiplexers	1

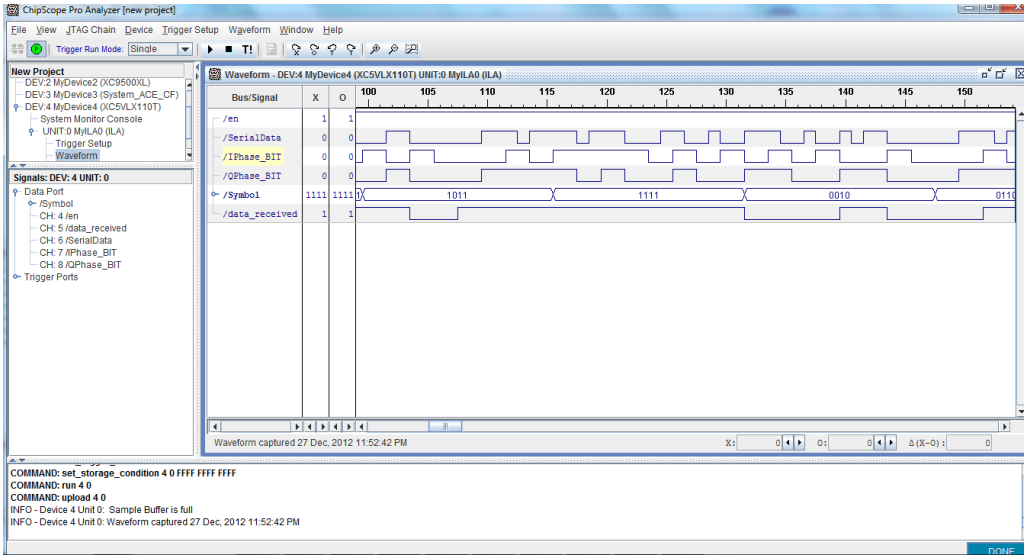


FIGURE 4.10: Chipscope Pro Internal signal for RNS based Baseband Receiver

- The baseband module is designed in hardware description language verilog HDL and simulated in mentor graphics modelsim simulator and the signal at each stage is analyzed.
- In FPGA implementation, similar to chapter 3 the synchronous clock circuitry is designed for 250 KHz, 10 MHz, and 1 MHz by taking 100 MHz board frequency from AH 15 PIN. Further, the implemented designs synthesis report along with some of internal signals of the design are also analyzed for verification.
- In XILINX power analysis, the total logic power consumption for RNS based baseband transceiver is found to be same as 0.45mW.

5

Conclusions and Future Scope of Work

This thesis presents the design and implementation of ZigBee transceiver for IEEE 802.15.4. It has been aimed to achieve a complete ZigBeee transceiver for short range wireless communication keeping in mind for military application. Each standard supporting short range wireless communication has different specifications and different applications. These days mobile communication has achieved wide applicability, but for application of short range communication in isolated area mobile communication is very difficult to implement. ZigBee transceiver provides a resilient technology to communicate in shorter range.

5.1 ZigBee Transceiver Design using FPGA

A FPGA design for ZigBee transceiver has been completed in this thesis. The development was completed through following steps

- Simulation of transceiver performance was carried out using Simulink. The desired signals of Simulink model of transceiver was analyzed during performance analysis.
- The baseband transceiver is described in hardware description language Verilog HDL for simulation in mentor graphics modelsim simulator.

- Following this the simulated design of transceiver was synthesized by using ISE design environment to implement on Virtex 5 FPGA. Further the board synthesis report and FPGA internal signals are analyzed. From analysis it is reported that the implemented design consumes 0.45 mW logic power at maximum clock frequency of 11.792 MHz and transportation delay from input to output is 3.264 ns.

In second phase of the design, a new proposed set of PN sequence is generated based on RNS which is used for baseband transmission and reception. Further the BER performance analysis of proposed RNS based PN sequence is compared with Pseudo Noise sequence for different noise conditions. From analysis it is seen that the RNS based receiver performs very similar to PN based ZigBee, however at low SNR the proposed RNS based coding provides better performance. The RNS based PN sequence is used as spreading code in transceiver implemented on Virtex 5 FPGA board in ISE design environment.

5.1.1 Design Discussion

Physical layer in ZigBee inter operates with the other upper layers of networking protocol such as MAC layer, Network layer and application layer etc. ZigBee devices used in upper layer are based on IEEE 802.15.4 standard operate in mesh networking topology with line of sight (LOS) communication. The underlying IEEE 802.15.4 standard provides strong reliability through different mechanisms at multiple layers. In line of this the design of the physical layer developed in this thesis is expected to work with other layers.

5.2 Limitation of work

The work reported in this thesis has certain limitations. some of the limitations are listed below.

- The thesis analyzed a baseband transceiver design suitable for 2.4 GHz RF band. It does not take care of other frequency bands which include 868 MHz and 915 MHz.

- The receiver assumes AWGN model for the channel. Multipath effect and fading have not been considered in this analysis.
- The clock design in this system has been developed on the FPGA hardware. There may be difficulties associated when the transceiver is interface with other subsystem having their independent clocks.

5.3 Future Scope

Wireless communication is a fast evolving field. Technology changes have been very rapid. In view of this and limitations of work in thesis following are some of the directions for future research.

- Designing a multi band ZigBee transceiver covering 868 MHz, 915 MHz and 2.4 GHz can be useful from system application point of view.
- The system RF design possess an important challenge in any hardware development. Integrating the proposed baseband transceiver with a RF stage would provide a complete hardware design.
- The last step in future work can be consideration of chip fabrication based on a complete design of a ZigBee system.

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